Research Migration Project

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Title of the circuit : Design and Simulation of a Clock-Gating Cell for Low-Power VLSI Systems using eSim

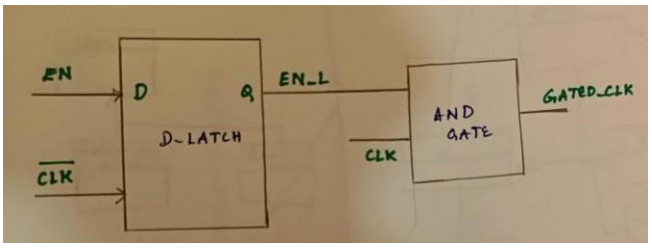
Description : Clock gating is an effective low-power technique used in VLSI systems to reduce dynamic power consumption by preventing unnecessary clock switching in idle circuit blocks. Since the clock signal has the highest switching activity, continuous toggling leads to significant power dissipation. A clock-gating cell operates by controlling the clock signal using an enable condition while ensuring glitch-free operation. This is achieved by sampling the enable signal through a level-sensitive latch when the clock is inactive and then combining the latched enable with the clock using a logic gate to generate a gated clock output. When enabled, the clock propagates normally, and when disabled, clock transitions are blocked, thereby reducing switching activity. In this work, a CMOS-based clock-gating cell is designed and simulated using eSim to demonstrate its functionality and suitability for low-power VLSI applications.

Reason to reproduce with eSim : The clock-gating cell is well suited for reproduction using eSim as it is a fundamental CMOS-based VLSI building block that can be accurately modeled and simulated at the transistor and logic levels. eSim provides an open-source platform with integrated schematic capture and simulation capabilities, making it ideal for verifying the functional correctness and timing behavior of clock-gating circuits. Reproducing this circuit in eSim has strong educational value, as it allows visualization of glitch-free clock control and power-saving concepts in synchronous digital systems. Additionally, implementing the clock-gating cell in eSim helps extend the availability of low-power VLSI design examples in an open-source environment.

Expected Outcome/outputs : Upon simulation, the clock-gating cell is expected to produce a gated clock output that correctly follows or blocks the input clock based on the enable signal. When the enable signal is asserted, the gated clock should toggle synchronously with the input clock, allowing normal operation of downstream circuits. When the enable signal is deasserted, the gated clock transitions should be suppressed, demonstrating effective clock disabling. The correctness of the circuit can be validated by observing glitch-free gated clock

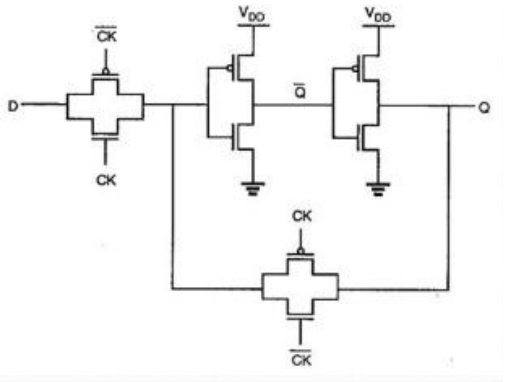
waveforms in transient simulations and verifying proper enable-controlled behavior, which confirms the functional operation of the clock-gating cell.

Circuit Diagram(s) :

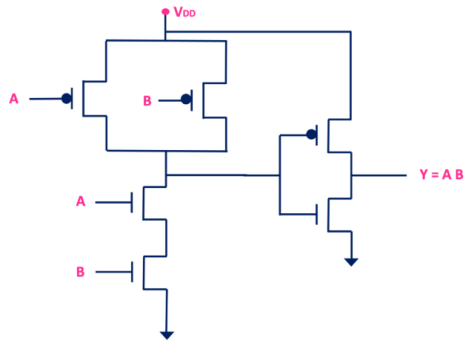


Signal	Description
CLK	Input clock signal (pulse source)
$CL\bar{K}$	Inverted clock (generated using inverter)
EN	Enable control signal
EN_L	Latched enable output
GATED_CLK	Output gated clock

D-Latch:



AND gate:

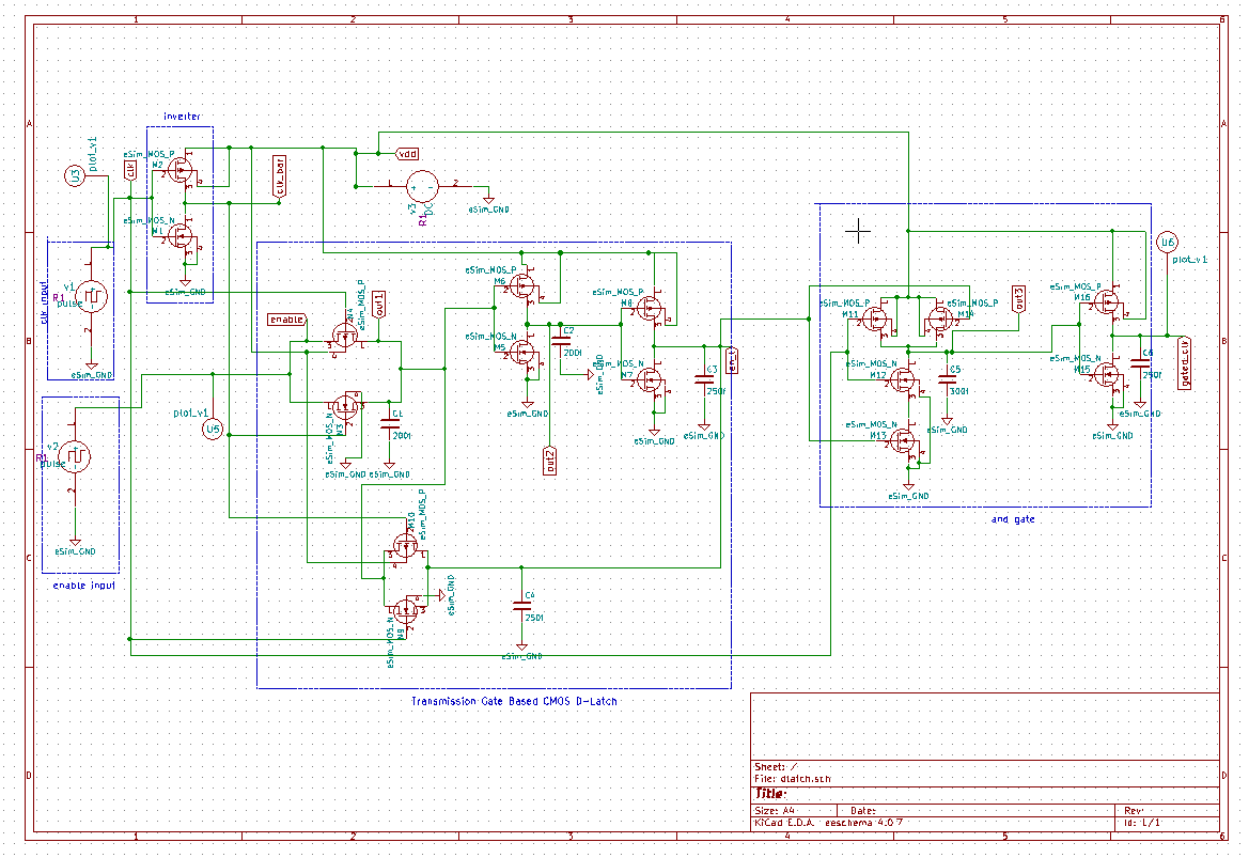


Behaviour Table:

$$GATED\_CLK = CLK \cdot EN_{\_latched}$$

Enable (EN)	Clock (CLK)	Gated Clock (GATED_CLK)
0	0	0
0	1	0
1	0	0
1	1	1

SCHEMATIC:



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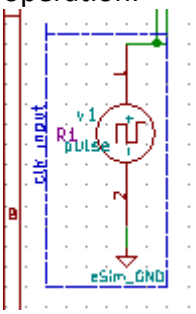
The proposed circuit implements a glitch-free clock gating cell at the transistor level using 180 nm CMOS technology. The schematic is organized into four functional stages: the clock input stage, the clock inversion stage, the transmission gate based D-latch, and the clock gating logic stage.

4.1 Clock Input Stage

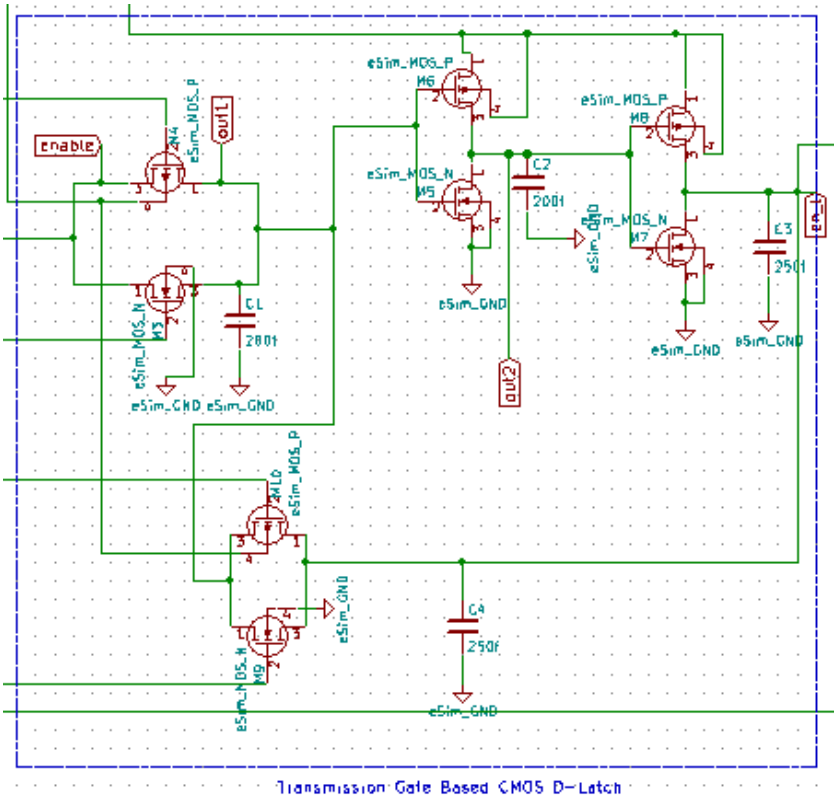
The clock signal is generated using a pulse voltage source operating at 1.8 V. This clock serves as the primary switching signal for the circuit. The non-inverted clock is applied directly to one input of the clock gating logic, while an inverted version of the clock, generated using a CMOS inverter, is applied to the control input of the transmission gate based D-latch. Proper rise and fall times are maintained to ensure realistic transient behavior consistent with 180 nm CMOS operation.



4.2 Transmission Gate Based D-Latch

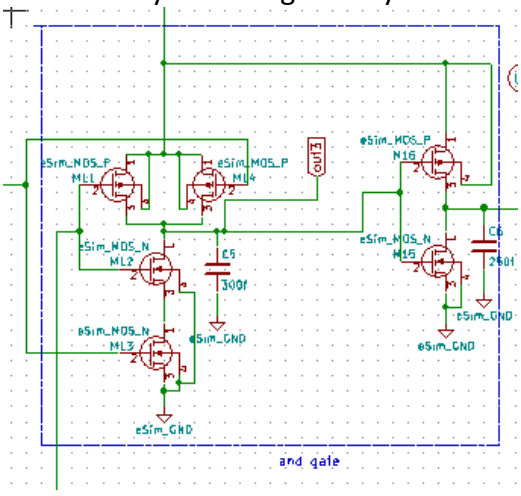
The enable signal is applied to a transmission gate based D-latch controlled by the inverted clock. When the inverted clock is high, the latch samples the enable input; when it is

low, the latch holds the sampled value.
A transmission gate latch is used instead of a simple pass-transistor latch to ensure full voltage swing without threshold voltage loss. The parallel NMOS and PMOS structure allows both strong ‘0’ and strong ‘1’ propagation, improving noise margin and signal integrity. This ensures that the enable signal is cleanly latched before being applied to the clock gating logic, thereby preventing glitches at the gated clock output.



4.4 Clock Gating Logic

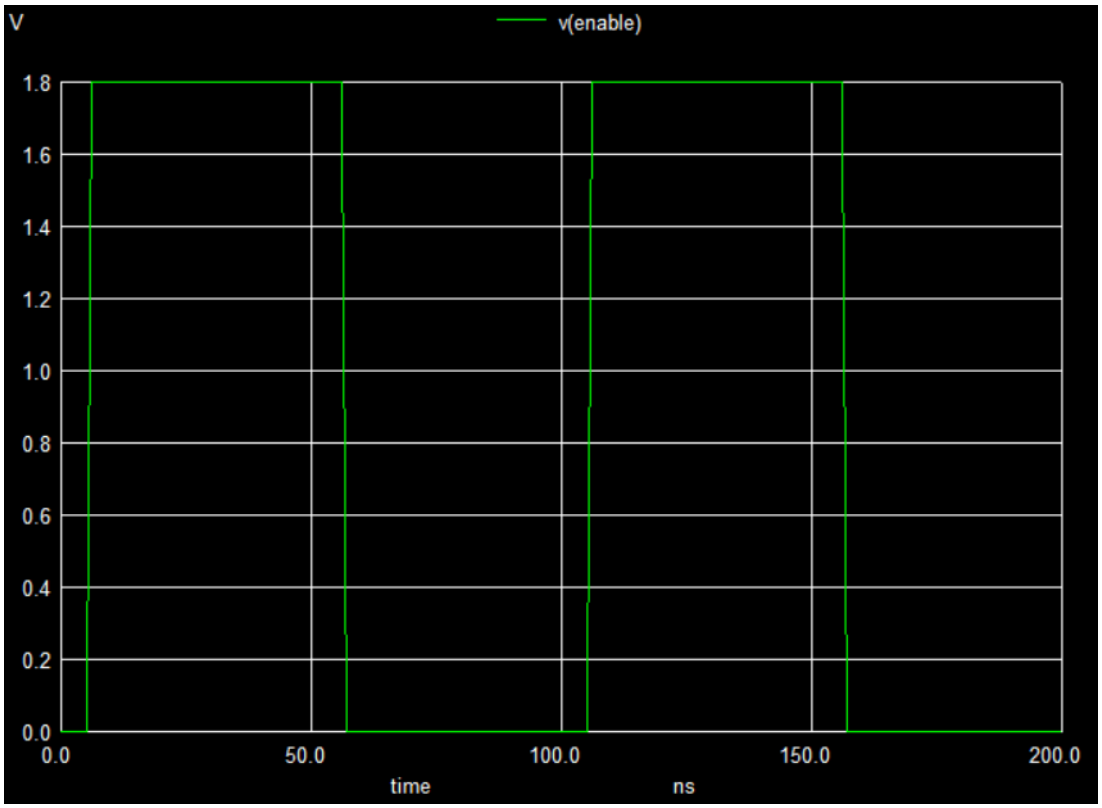
The output of the D-latch is applied to one input of a static CMOS AND gate configuration, while the original (non-inverted) clock is applied to the other input. The AND gate produces the final gated clock output.
When the latched enable signal is high, the AND gate allows the original clock to propagate to the output. When the latched enable signal is low, the output remains at logic low, effectively suppressing clock transitions. This controlled propagation of the clock signal reduces unnecessary switching activity in downstream circuitry.



Capacitors are placed at the output of each stage to model parasitic capacitances, interconnect loading, and fanout effects present in practical integrated circuits. Including these capacitive loads enables realistic transient analysis of propagation delay, rise and fall times, and overall switching behavior of the gating cell under non-ideal conditions.
All transistors are implemented with a channel length of 0.18 µm, and PMOS devices are sized approximately twice the width of NMOS devices to achieve balanced switching characteristics.

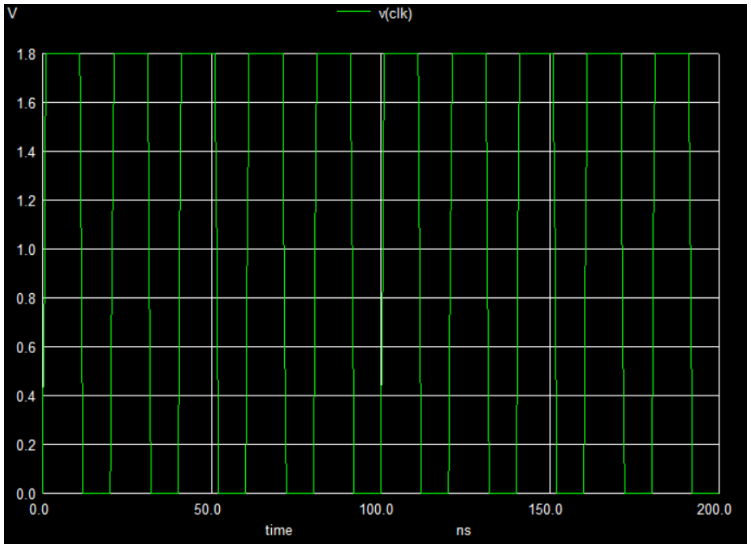
RESULTS:

Fig 1: Enable Signal Waveform



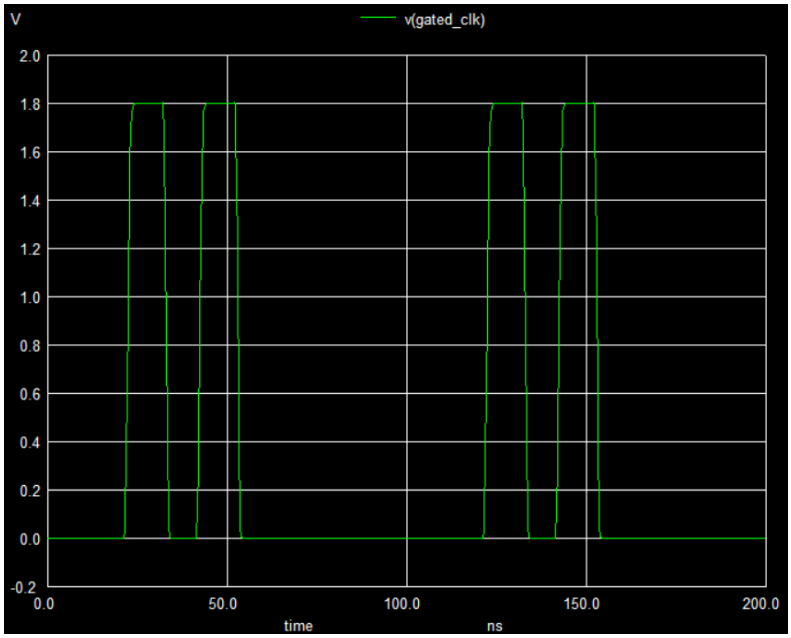
The enable waveform switches between 0 V and 1.8 V, controlling whether the clock is allowed to propagate through the gating logic. High levels permit clock transmission, while low levels suppress the gated clock output.

Fig 2: Input Clock Waveform



The clock waveform shows periodic switching between 0 V and 1.8 V, serving as the primary timing reference for the clock gating circuit. This signal is applied directly to the AND gate and inverted to control the D-latch operation.

Fig 3: Gated Clock Output Waveform



The gated clock output remains at 0 V when the enable signal is low, indicating that clock propagation is successfully suppressed. When the enable signal is high, the gated clock follows the input clock waveform, confirming correct glitch-free clock gating operation.

REFERENCES:

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