Research Migration Project

https://esim.fossee.in/research-migration-project

The Research Migration Project is an initiative of FOSSEE, IIT Bombay that promotes the use of eSim for reproducing published research circuits originally implemented using proprietary simulation tools. The objective is to migrate these validated designs to eSim to build an open source resource database.

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Title of the circuit : Implementation of Low-Power Wallace Tree Multiplier Using eSim Circuit Simulator

Theory/Description :

Multipliers are critical components in digital systems, but conventional multiplier architectures consume high power and area because partial products are reduced using complex adder structures with large gate counts and high switching activity. In particular, traditional Wallace tree multipliers rely on conventional full adders containing multiple XOR gates, which increases delay and power consumption, making them less efficient for modern low-power digital applications.

To overcome this problem, this project implements an optimized Wallace Tree Multiplier in eSim by replacing the conventional full adders in the reduction stage with a modified low-power full adder using multiplexers and fewer logic gates. This approach reduces switching activity, hardware complexity, and delay while maintaining correct multiplication results. The proposed circuit therefore provides a more power-efficient and faster multiplier suitable for modern digital and embedded system applications.

Reason to reproduce with eSim :

This circuit is suitable for simulation using eSim as it supports gate-level digital design and allows easy verification of complex arithmetic circuits. Being open-source and educational, eSim helps visualize and validate the optimized Wallace Tree Multiplier and clearly demonstrate the improvements in logic efficiency and performance over conventional designs.

Expected Outcome/outputs :

When simulated, the circuit is expected to correctly perform unsigned binary multiplication of two 4-bit input numbers and produce an 8-bit output. The multiplier should generate correct results for all valid input combinations. The optimized reduction stage using the modified full adder is expected to demonstrate reduced logic depth and efficient signal propagation compared to conventional designs.

Correct functionality will be validated by comparing the output product with the expected mathematical multiplication of the input operands.

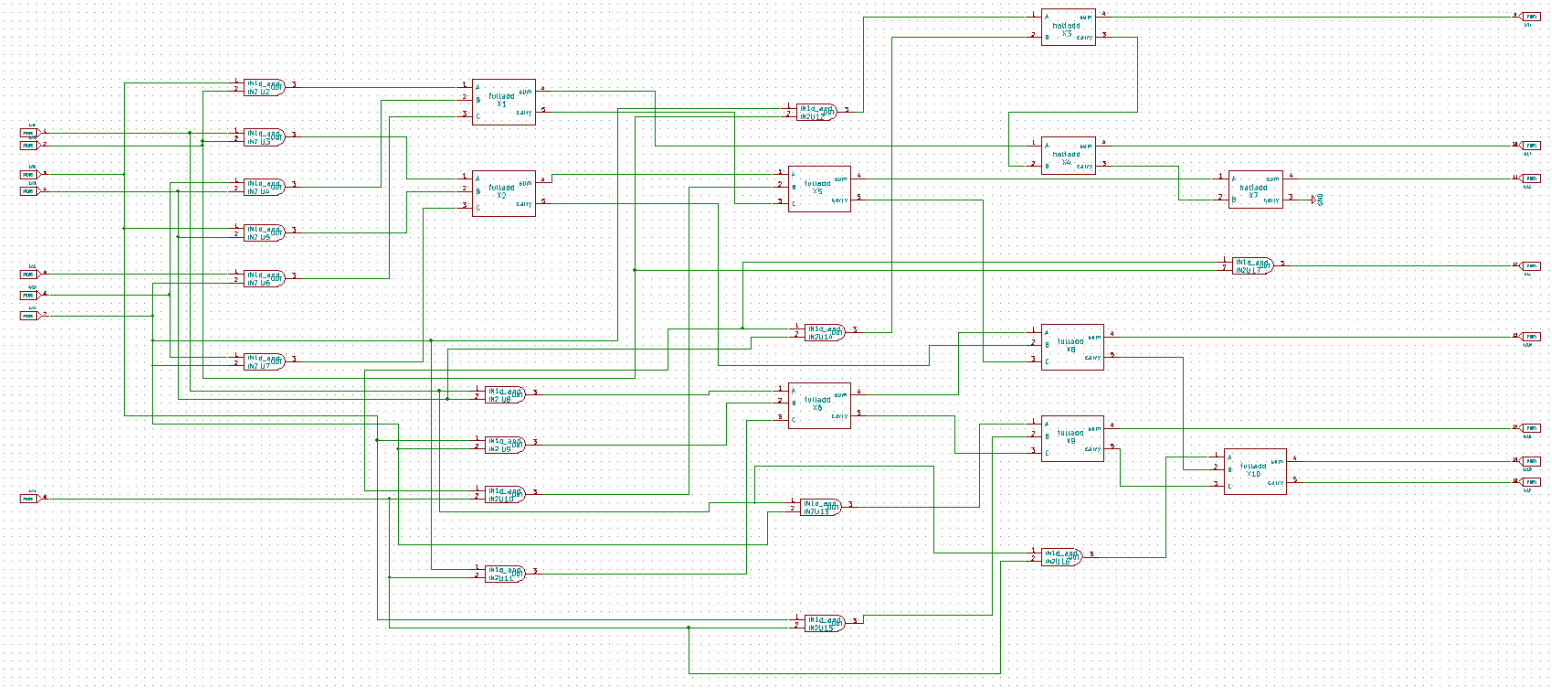
Circuit Diagram(s) :

The circuit diagram includes:

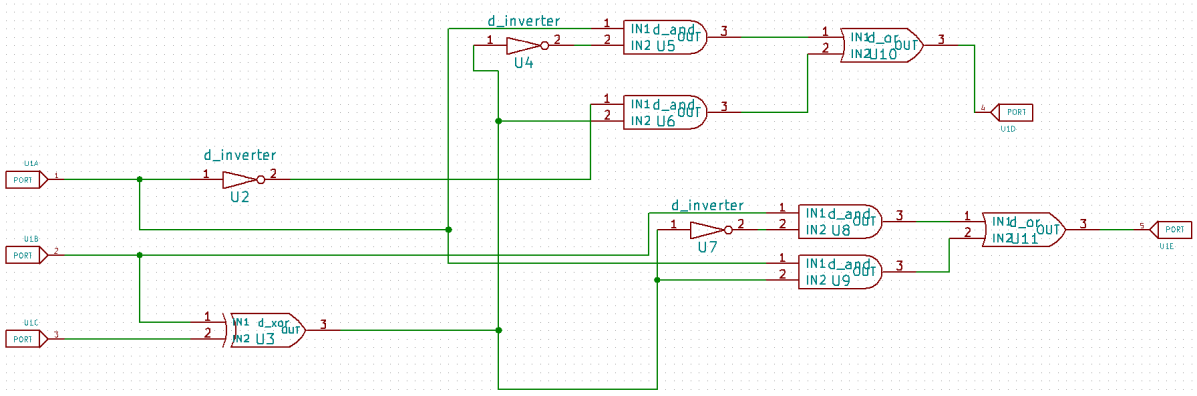
- AND gates for partial product generation.
- Modified full adders using multiplexers and XOR gates for Wallace tree reduction.
- Half adders where required.
- Final addition stage to produce the output product.

The schematic clearly shows all logic gate connections, signal paths, and labeled inputs and outputs, enabling complete understanding and evaluation of the design.

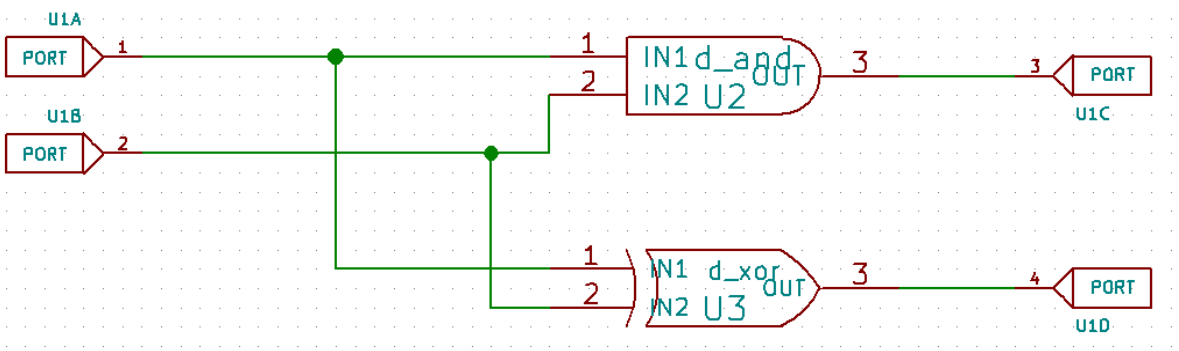
Schematic Diagram:



img.1 4x4 Wallace Tree Schematic Diagram

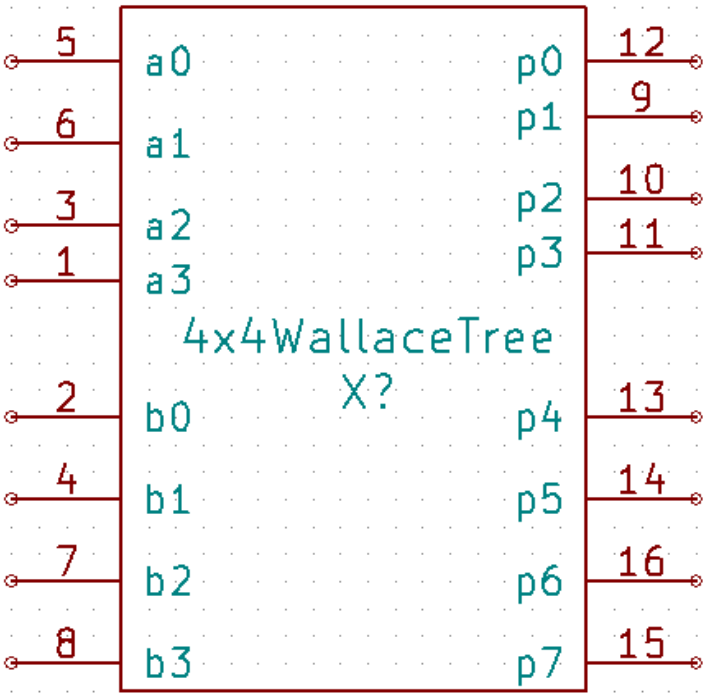


img.2 Optimized Full Adder Schematic Diagram

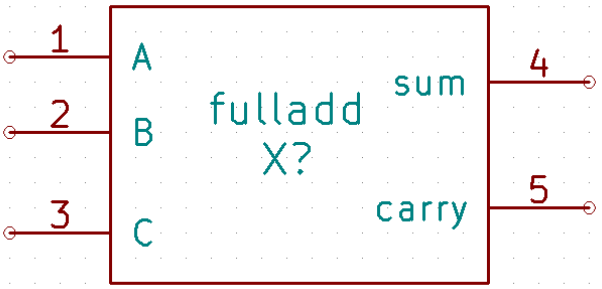


img3. Hall Adder Schematic diagram

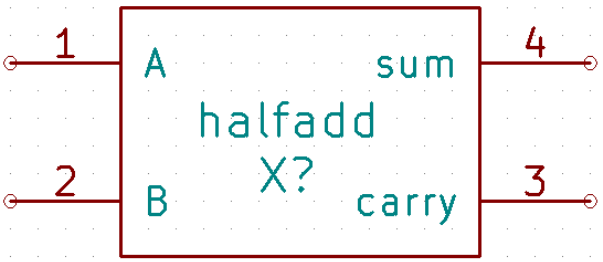
Subcircuit Diagram:



img.4 4x4Wallace Tree Subcircuit



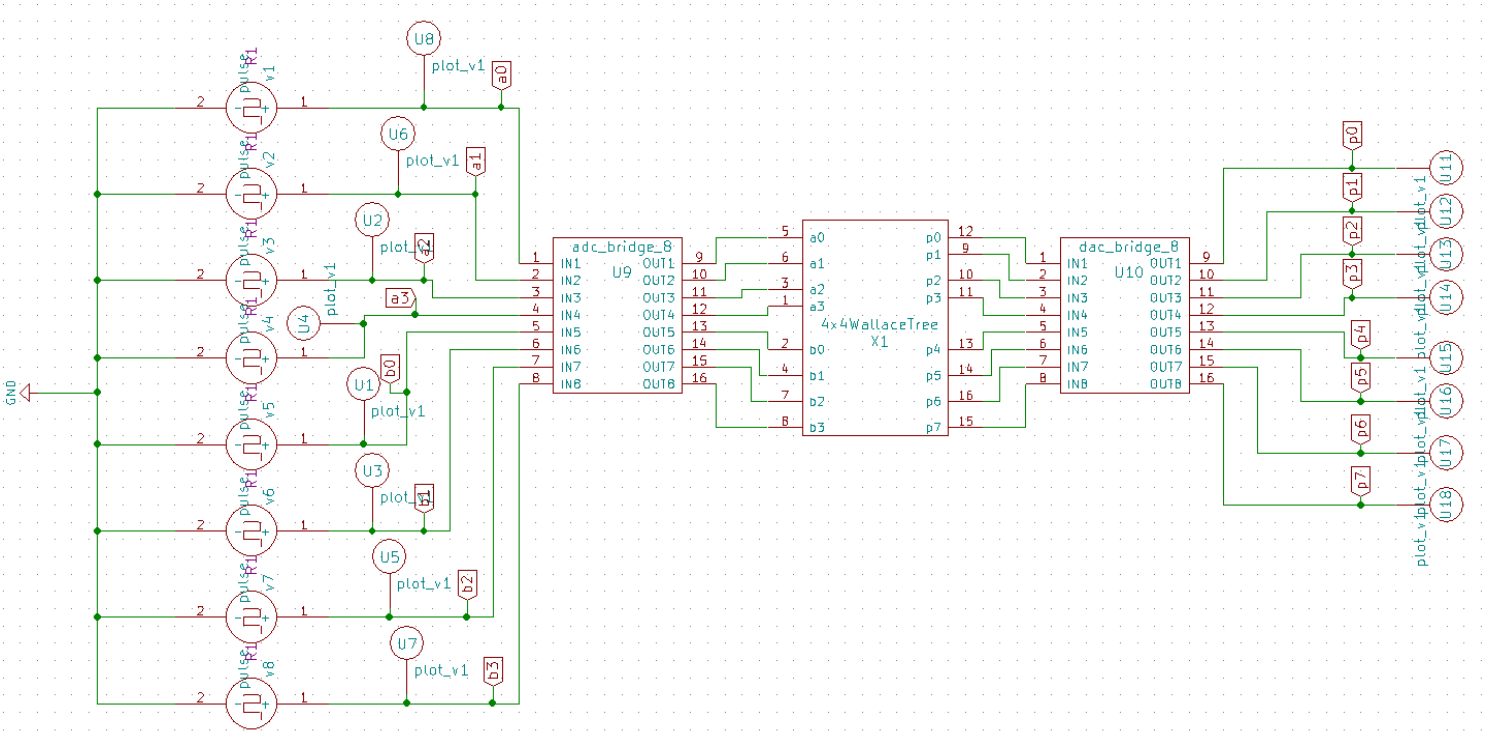
img.5 Full Adder Subcircuit



img.6 Half Adder Subcircuit

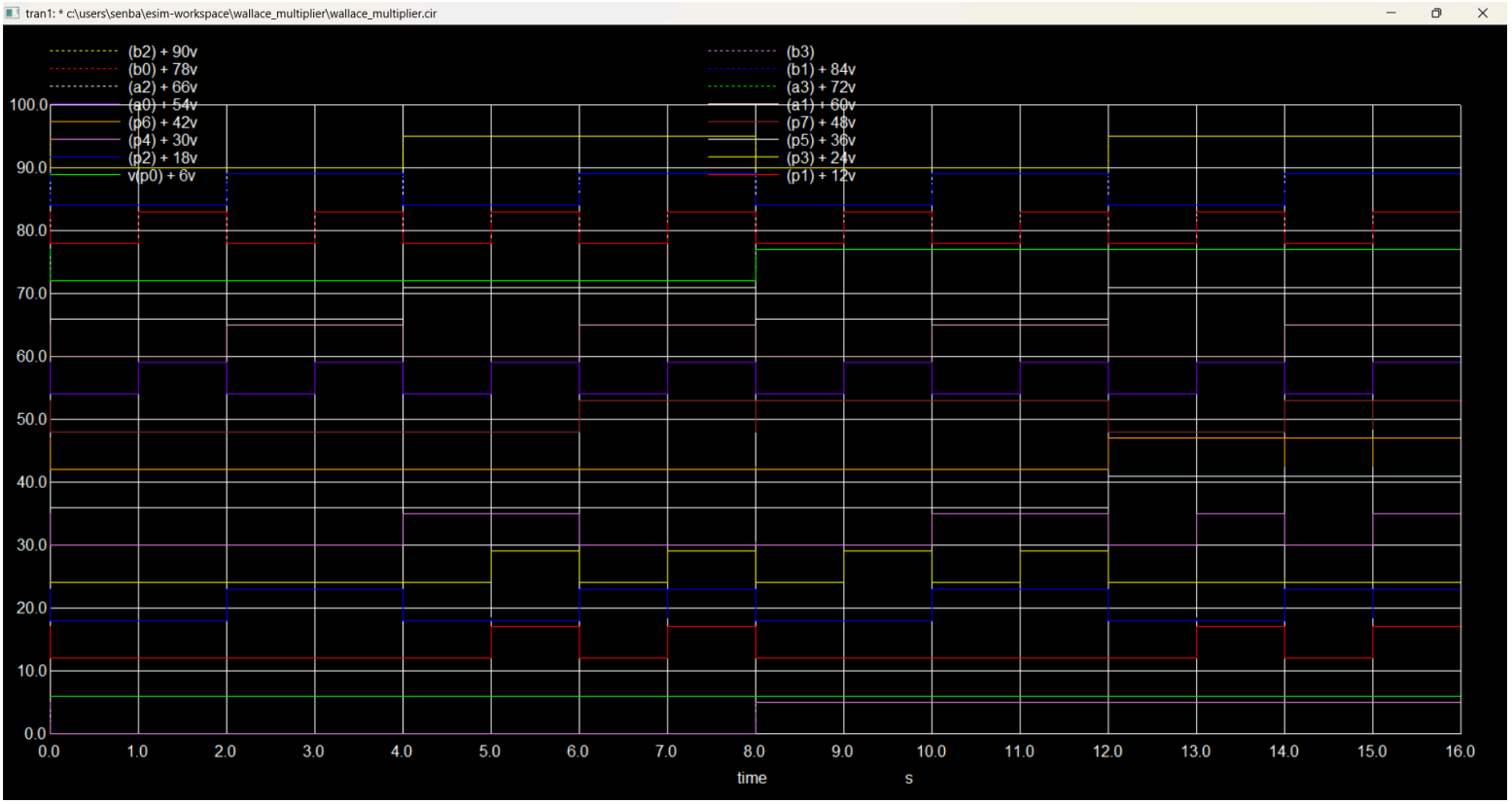
Test Circuit:

The test circuit is designed to apply different combinations of input values to the Wallace Tree Multiplier and verify its functionality through simulation. By providing various binary inputs and observing the corresponding output product, the correctness of the multiplier operation is validated. The simulated results are compared with expected multiplication values to ensure accurate circuit behavior.



img.7 Test Circuit

Simulation Output:



img.8 Stacked Simulation Output

Truth Table:

Truth Table – 4-Bit Wallace Tree Multiplier			
a3 a2 a1 a0	b3 b2 b1 b0	p7 p6 p5 p4 p3 p2 p1 p0	Result
0000	0000	00000000	0 × 0 = **0**
0001	0010	00000010	1 × 2 = **2**
0011	0010	00000110	3 × 2 = **6**
0101	0100	00010100	5 × 4 = **20**
0111	0011	00010101	7 × 3 = **21**
1001	0110	00110110	9 × 6 = **54**
1110	1010	11101000	14 × 10 = **140**
1111	1111	11100001	15 × 15 = **225**

img.9 Truth Table

Research Paper/Journal/etc. :

Title : Low Power Wallace Tree Multiplier Using Modified Full Adder
Author : Kokila Bharti Jaiswal, Nithish Kumar V, Pavithra Seshadri, Lakshminarayanan
Page No. : 4
Link : [Low power wallace tree multiplier using modified full adder | IEEE Conference Publication | IEEE Xplore]

Source/Reference(s) :

- C. Wallace, *A Suggestion for a Fast Multiplier*, IEEE Transactions on Electronic Computers.
- eSim Circuit Simulation Platform – FOSSEE Project, IIT Bombay.
- Digital Design textbooks and lecture notes on arithmetic circuits.