Research Migration Project

https://esim.fossee.in/research-migration-project

The Research Migration Project is an initiative of FOSSEE, IIT Bombay that promotes the use of eSim for reproducing published research circuits originally implemented using proprietary simulation tools. The objective is to migrate these validated designs to eSim to build an open source resource database.

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Title of the circuit: Implementation of Synchronous Serial-In Serial-Out (SISO) Shift Register Using D Flip-Flops in eSim Circuit Simulator

Theory/Description :

Shift registers are fundamental sequential circuits used for data storage and transfer in digital systems. A Serial-In Serial-Out (SISO) shift register allows data to be entered into the system one bit at a time and retrieved in the same serial manner after a fixed number of clock pulses. Such registers are widely used in serial communication, timing control, and data synchronization applications.

In this project, a synchronous SISO shift register is implemented using D flip-flops in the eSim circuit simulator. The circuit consists of cascaded D flip-flops, all driven by a common clock signal to ensure synchronous operation. The serial data input is applied to the D input of the first flip-flop, while the Q output of each flip-flop is connected to the D input of the subsequent flip-flop. On every rising edge of the clock, the input data is shifted from one flip-flop to the next.

The serial output is taken from the Q output of the last flip-flop in the chain. A reset signal is used to initialize all flip-flops to a known state before operation. The implemented circuit demonstrates correct bit-by-bit shifting behavior and serves as a basic building block for more complex digital systems.

Reason to Reproduce with eSim:

The synchronous Serial-In Serial-Out (SISO) shift register is a fundamental digital building block widely used in data storage, data transfer, and serial communication systems. Reproducing this circuit using eSim, an open-source circuit simulation tool, enables transparent verification of its operation at the gate and circuit level, which is not easily achievable using proprietary EDA tools.

ESim allows the D flip-flop to be implemented using basic logic gates, providing deeper insight into the internal working of the shift register and its timing behavior. This approach enhances educational value by bridging the gap between theoretical concepts and practical circuit implementation. Additionally, eSim's NGSpice-based simulation environment enables accurate waveform analysis and validation of synchronous operation without relying on commercial software.

By migrating the design to eSim, the circuit becomes accessible to students and researchers, promoting open-source learning, reproducibility of results, and cost-effective digital circuit design.

Expected outcome/output:

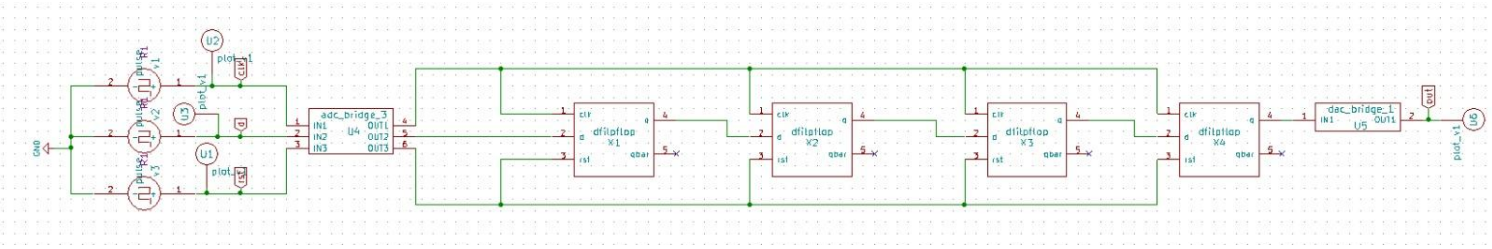
When the synchronous SISO shift register is simulated in eSim, the circuit is expected to operate correctly on each active clock edge. Upon asserting the reset signal, all flip-flop outputs are cleared to logic 0, initializing the shift register to a known state. When the reset is de-asserted, serial data applied at the input is shifted through the register one bit per clock pulse.

The serial input appears at the output after a number of clock cycles equal to the number of flip-flop stages used in the shift register. During normal operation, the output remains stable between clock edges, confirming synchronous behavior. The simulation waveforms should clearly demonstrate proper data shifting, correct reset functionality, and stable output transitions synchronized with the clock.

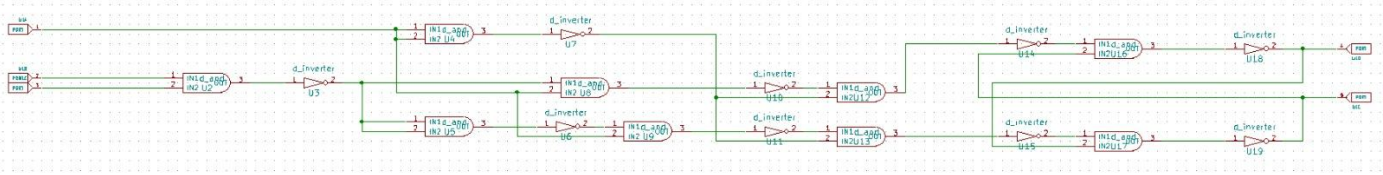
Circuit Diagram(s):

The circuit consists of:

- D flip-flops connected in cascade,
- A common clock signal applied to all flip-flops for synchronous operation,
- Serial data input connected to the first flip-flop,
- Serial data output taken from the last flip-flop,
- Reset signal for initialization of the flip-flops.

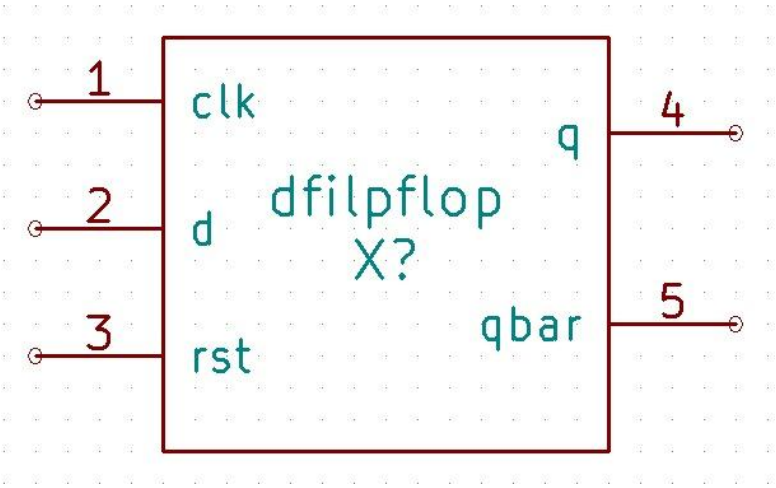


Img1. 4 Bit Synchronous Serial In Serial Out Schematic Diagram



Img2. D Flip Flop Schematic Diagram

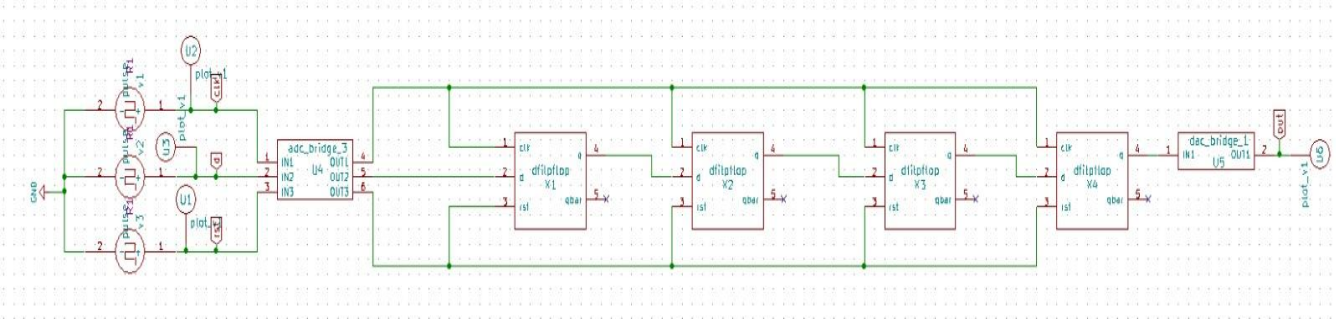
Subcircuit Diagram:



Img3. Symbol of D Flip Flop

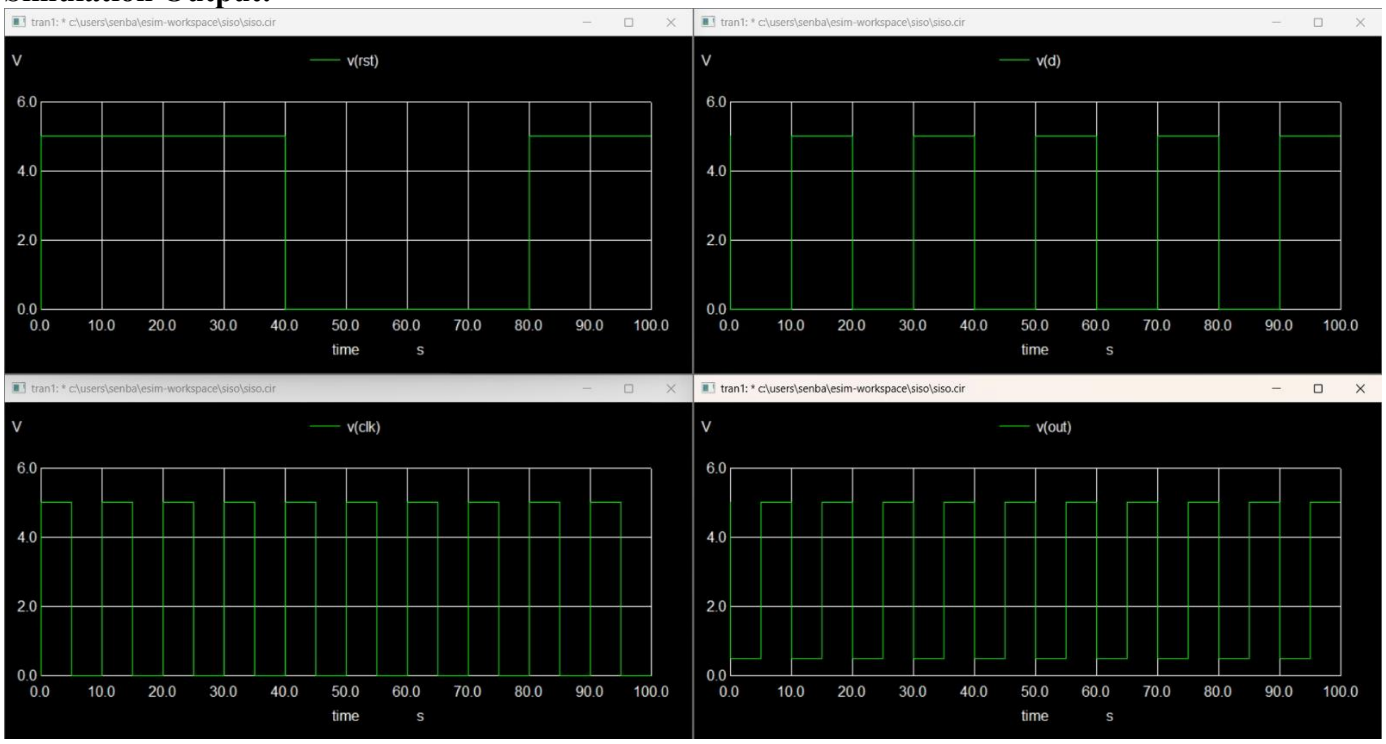
Test circuit:

The test circuit for the synchronous Serial-In Serial-Out (SISO) shift register in eSim consists of a clock source, a reset source, and a serial data input source connected to the gate-level SISO shift register built using D flip-flops. The clock signal is applied commonly to all flip-flops to ensure synchronous operation, while the reset signal initializes all stages of the shift register to logic zero. A pulse or digital source is used to apply serial input data to the first flip-flop, and the serial output is taken from the last flip-flop stage. Output probes are connected to the intermediate and final outputs to observe the shifting of data bits on each clock edge, thereby verifying correct reset operation and synchronous data transfer through the shift register.



Img4. Test Circuit

Simulation Output:



Img5. Simulation Output of Serial In Serial Out

Truth Table:

rst	Clock (↑)	d	out (next)
1	↑	0	0
1	↑	1	0
0	↑	0	0
0	↑	1	1
0	No ↑	X	Previous out

Img6. Truth Table

Source/Reference(s):

1. Rapartiwar, Namrata, and Vinod Kapse. "Design of Serial in Serial out And Serial in Parallel out Shift Register Using Double Edge Triggered D Flip Flop." *International Journal of Emerging Technology and Advanced Engineering (IJETAE)* 4.7 (2014): 505-508.