Design and Simulation of a Voltage-to-Time Converter With ReLU Transfer Curve Using eSim

eSim Research Migration Project

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Abstract

This work presents the reproduction of a Voltage-to-Time Converter (VTC) with an inherent Rectified Linear Unit (ReLU) transfer characteristic using the open-source eSim platform in 180-nm CMOS technology. The circuit architecture is derived from a recent IEEE SSCS publication, where switched-capacitor sampling, a transconductance stage, and evaluation logic generate output pulses whose widths represent the input voltage. Transient simulations were carried out to observe the internal node voltage $V_{CO}$and the output V_{out}. The obtained waveforms closely follow the behavior reported in the reference work, even though a different technology node is used. This confirms that the essential operating principle of the VTC is successfully reproduced in eSim.

1 Introduction

Energy-efficient analog and mixed-signal circuits are becoming increasingly important for neural-network hardware accelerators. Instead of converting signals repeatedly between voltage and digital domains, Voltage-to-Time Converters encode information directly in pulse widths, which can significantly reduce power consumption.

The SSCS Student Circuit Contest recently reported a highly optimized VTC implemented in 22-nm FDSOI technology that produces ReLU-like transfer characteristics suitable for analog neural processing.

The aim of this project is to recreate that circuit using open-source tools under the FOSSEE Research Migration initiative. The design is implemented in eSim with 180-nm CMOS models. Although the technology node is different, the primary objective is to verify that the **functional behavior**—especially the ReLU-style pulse-width modulation—matches the published results.

2 Circuit Description and Working Principle

The reproduced VTC consists of four main parts:

- an input sampling network controlled by the SMPL signal,
- a switched-capacitor transconductance (G_m) stage,

- an evaluation block activated by the EVAL signal, and

- a CMOS inverter that generates the final output V_{out}.

During the sampling phase, the input voltage is stored on a capacitor. When the evaluation phase begins, the stored voltage is compared with device thresholds.

If the input is small, the discharge path remains inactive and no output pulse is produced—representing the zero region of the ReLU function. When the input exceeds the effective threshold, the $G_m$stage discharges the internal node V_{CO}. Once this node reaches a switching level, the output pulse is terminated.

As a result, higher input voltages generate longer pulses at the output, creating a time-domain representation of the ReLU characteristic.

3 Implementation Methodology in eSim

The circuit was implemented in eSim following these steps:

- Technology Choice: All MOSFETs were simulated using available 180-nm CMOS models.
- Schematic Capture: The complete VTC—sampling switches, capacitors, transconductance stage, evaluation network, and output inverter—was recreated in KiCad using eSim libraries.
- Clock Generation: SMPL and EVAL control pulses were applied using ideal voltage sources to replicate the two-phase operation described in the reference design.
- Simulation Setup: Transient analysis was carried out in Ngspice to observe time-domain behavior.
- Waveform Comparison: The simulated $V_{CO}$and V_{out}signals were compared with the transient plots presented in the SSCS publication, especially Figure 2.

4 Results and Discussion

The transient simulation results clearly show that the internal node voltage V_{CO}follows the same qualitative trend as in the reference work. During evaluation, V_{CO}discharges with a slope determined by the transconductance stage and capacitor values, and the discharge stops once the switching condition is reached.

The corresponding V_{out}waveforms demonstrate well-defined pulses that start and end at appropriate instants. For lower operating points, no output pulse is generated. As the effective input increases, the pulse width grows steadily—exactly as expected from a ReLU-type voltage-to-time mapping.

Although the original circuit was implemented in a 22-nm FDSOI process, the present work uses a 180-nm technology. Because of this, slower edges, slightly different voltage levels,

and minor timing variations are observed. These differences arise from higher parasitic capacitances and reduced device speed in the older node.

Despite this, the **overall functional behavior of both V_{CO} and V_{out}** closely resembles the SSCS Figure 2 results. The correct start-and-stop pulse generation and monotonic increase in pulse width confirm that the underlying VTC operation has been successfully reproduced in eSim.

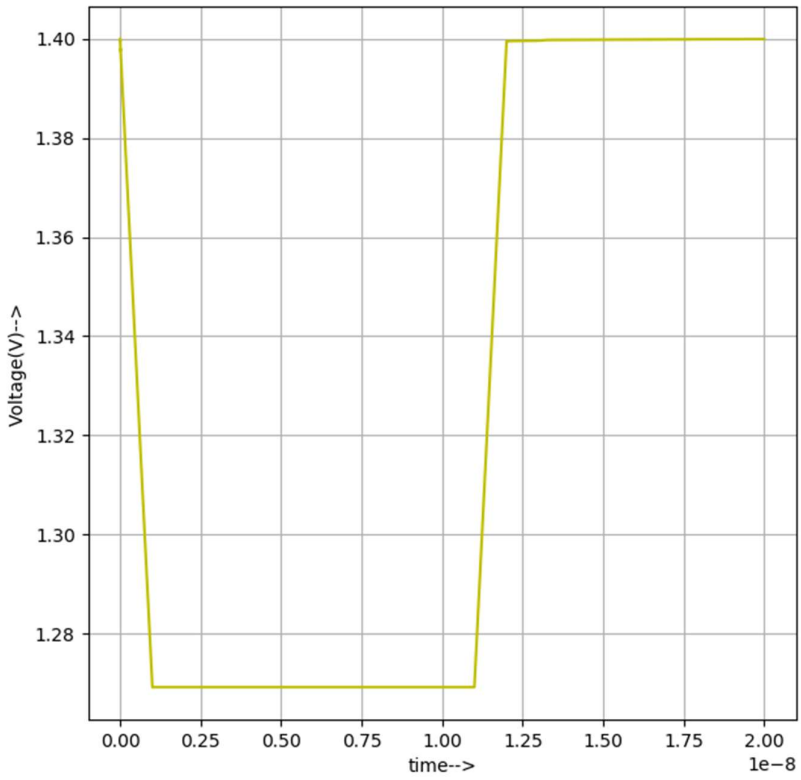

Figure 1: Vin

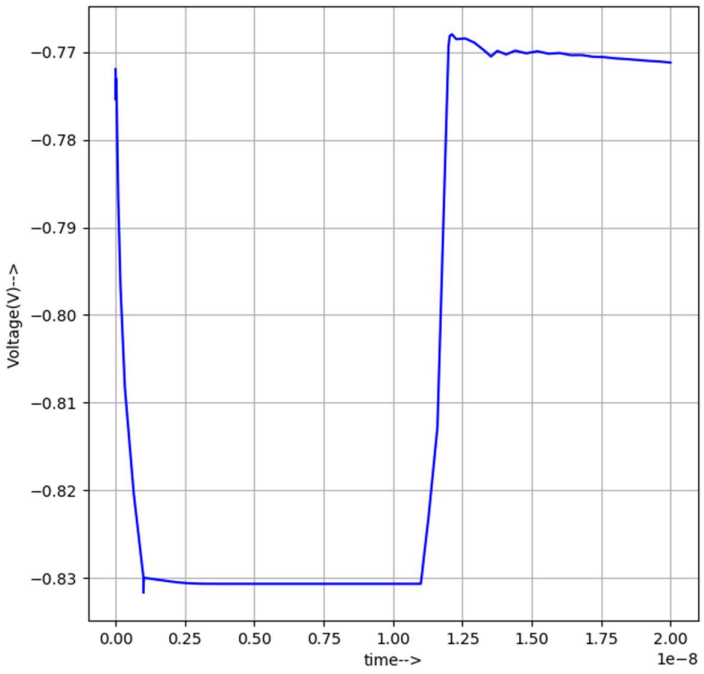

Figure 2: SMPL

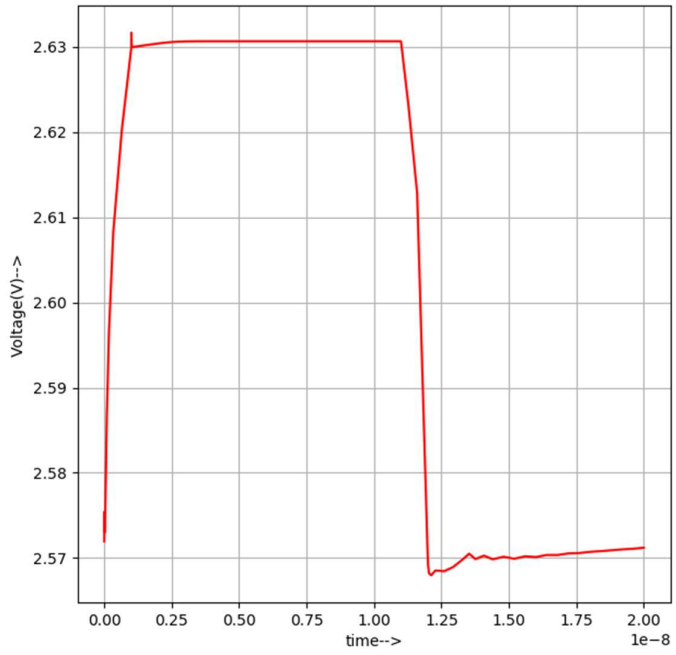

Figure 3: Vco vs time

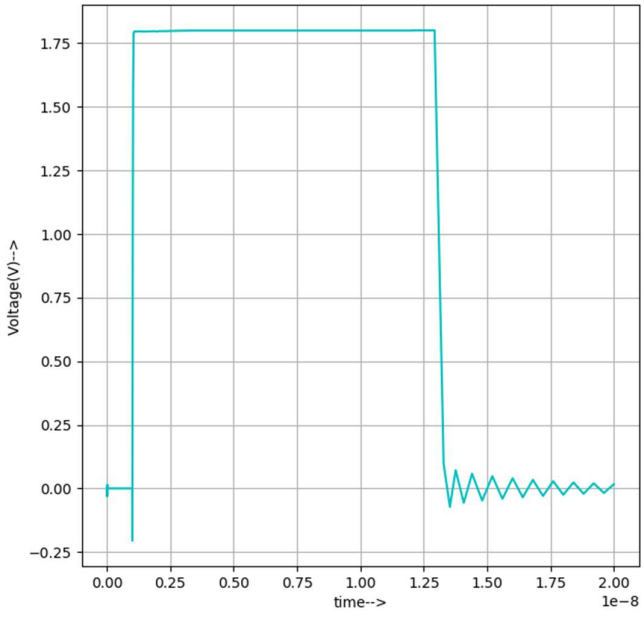

Figure 4: Vout Vs Time

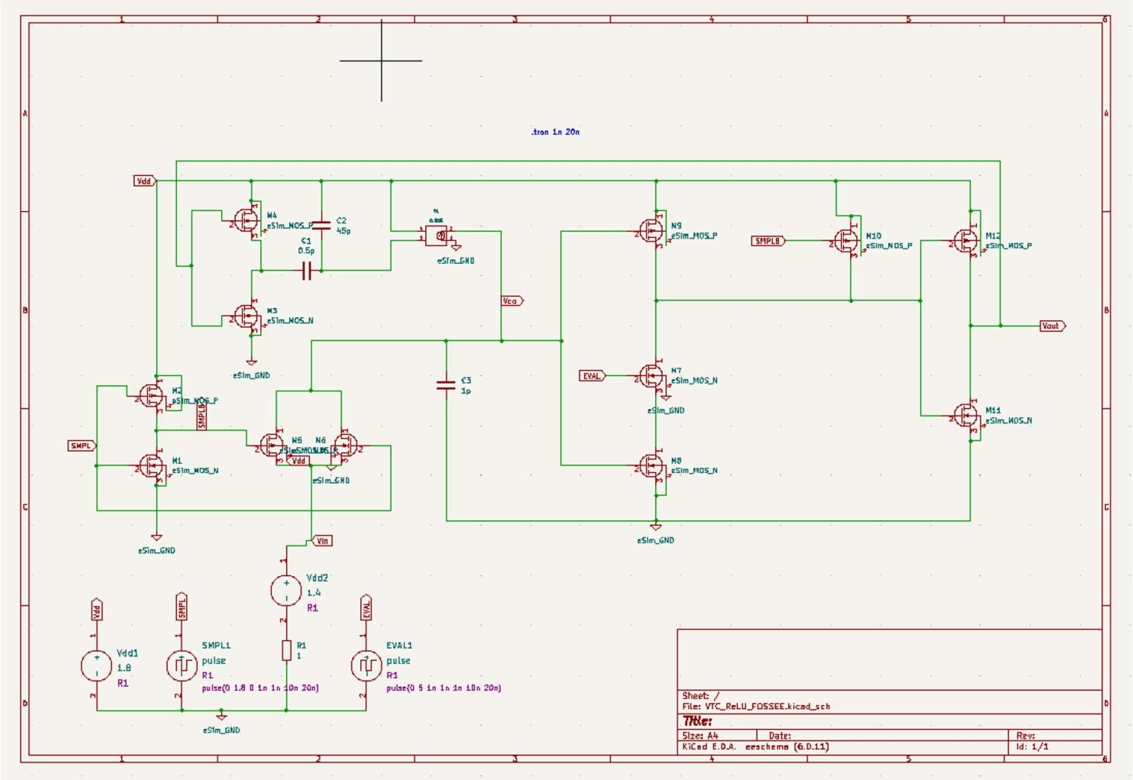

Figure 5: Schematic

5 Conclusion

This project successfully recreated an SSCS-reported Voltage-to-Time Converter with ReLU transfer characteristics using the open-source eSim platform and 180-nm CMOS models. Even with a different technology node, the simulated waveforms match the qualitative behavior of the reference design, including threshold-dependent pulse generation and proportional pulse-width variation. The strong agreement between the reproduced results and the published transient responses validates the circuit migration and demonstrates that advanced analog neural-inspired circuits can be studied and verified using open-source tools.

References

1. Jakob Finkbeiner, “An Energy-Efficient Voltage-to-Time Converter With Built-in ReLU Activation Function in 22-nm FDSOI,” *IEEE Solid-State Circuits Magazine*, Winter 2025. DOI: 10.1109/MSSC.2024.3490212.

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