

The Research Migration Project is an initiative of FOSSEE, IIT Bombay that promotes the use of eSim for reproducing published research circuits originally implemented using proprietary simulation tools. The objective is to migrate these validated designs to eSim to build an open source resource database.

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Title of the circuit : Analysis of Low-Power Dynamic Comparator Architectures

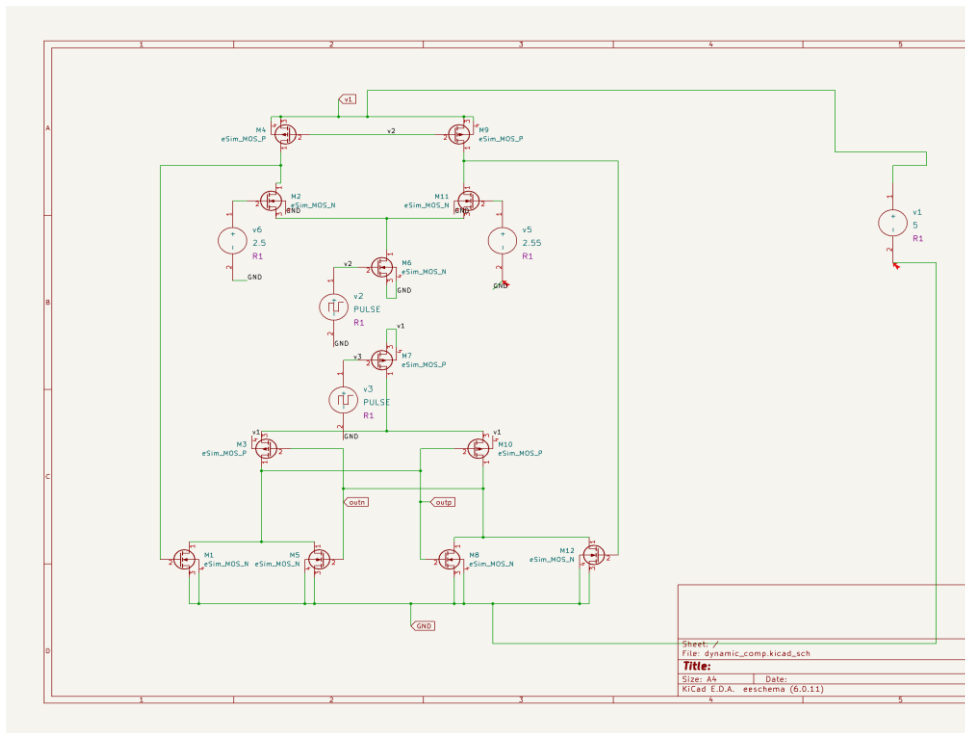
1. Theory/Description : *This project investigates the design and simulation of conventional and two-stage dynamic comparators in 130 nm CMOS technology. Functional behavior, clocked operation, and regenerative latch action are analyzed using transient simulations. Results demonstrate improved speed, gain, and output stability with the cross-coupled latch architecture.*

The paper reports that power dissipation varies significantly with the width of the cascade transistors. By sweeping the transistor width in 130 nm technology, the authors observe a minimum power dissipation when the width of the cascade transistors is 0.44 μm . This result demonstrates that careful transistor sizing plays a crucial role in reducing dynamic power consumption and that the proposed cascade dynamic comparator is more power-efficient than the conventional dynamic comparator.

2. Reason to reproduce with eSim : The dynamic comparator was reproduced and simulated on the eSim platform to enable open-source, SPICE-based verification of circuit functionality. eSim provides an accessible environment for schematic capture and transient analysis, allowing validation of comparator operation, clocked behavior, and regeneration without reliance on proprietary EDA tools.

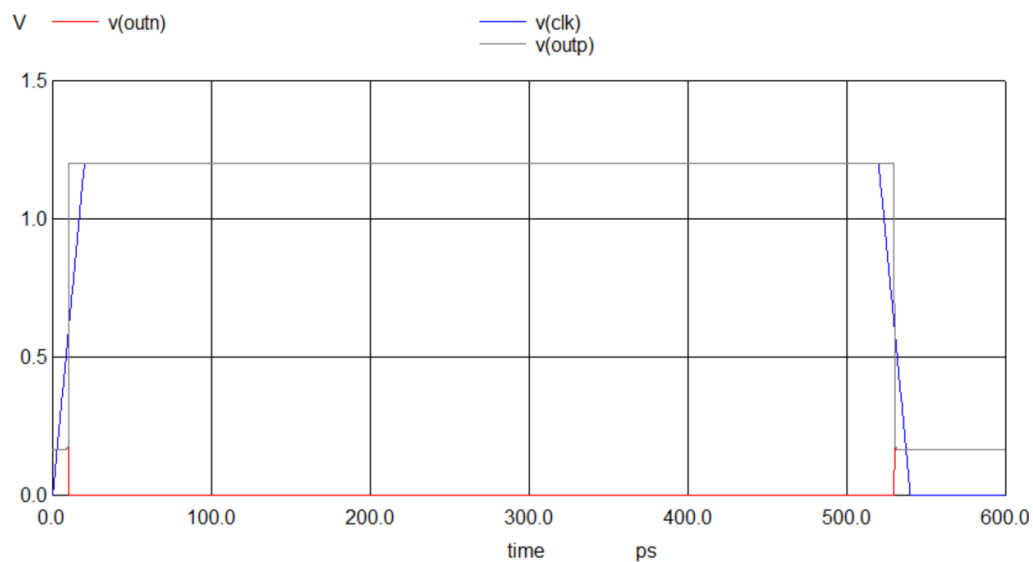
3. Comparator Architectures and Methodology

3.1 Conventional Dynamic Comparator with cascade transistors



Observations and results:

- The outputs show partial voltage separation, but do not reach full logic levels and the voltage difference increases slowly during the evaluation window.



- In published literature, the pre-latch waveforms often appear smooth and slanted. *However, exact reproduction of these waveforms was not achieved in this work due to the following reasons:*
 - Use of simplified Level-1 MOS models instead of BSIM3/BSIM4
 - Ideal clock and voltage sources in NGSPICE
 - Lack of noise modelling

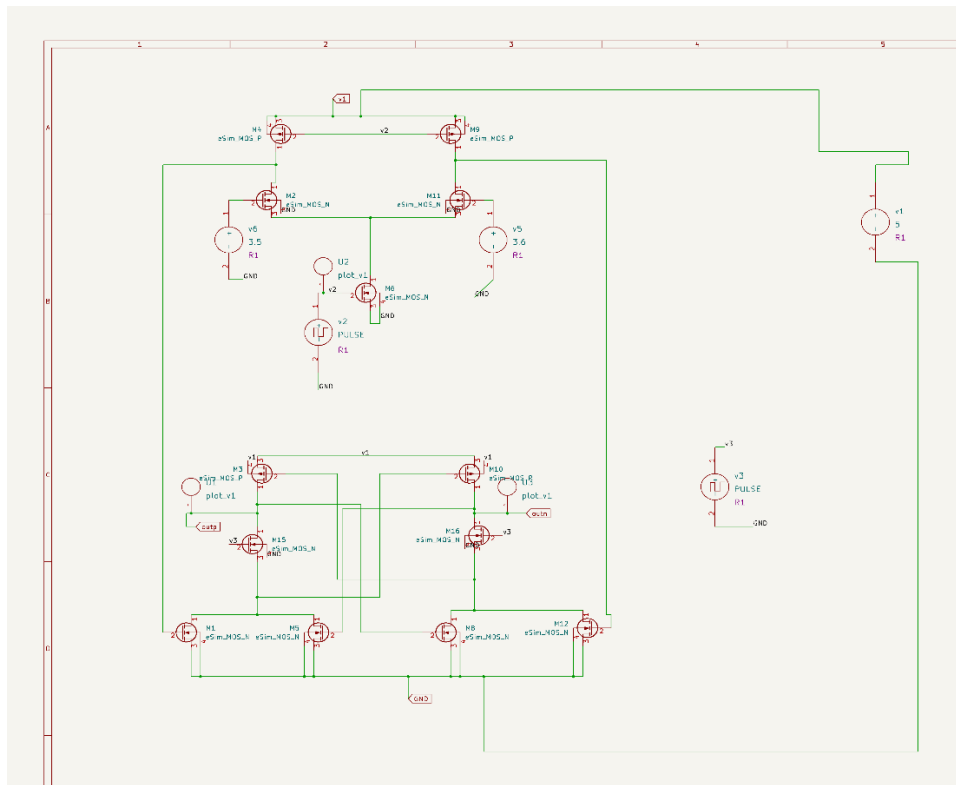
- This behavior is expected for a dynamic comparator without a regenerative latch, as the differential pair alone cannot provide strong positive feedback.

3.3 Two-Stage Dynamic Comparator with Cross-Coupled Latch

Single-stage dynamic comparators often suffer from limited output voltage swing and reduced noise immunity. To address this, the paper introduces a two-stage architecture by adding a cross-coupled latch as the second stage.

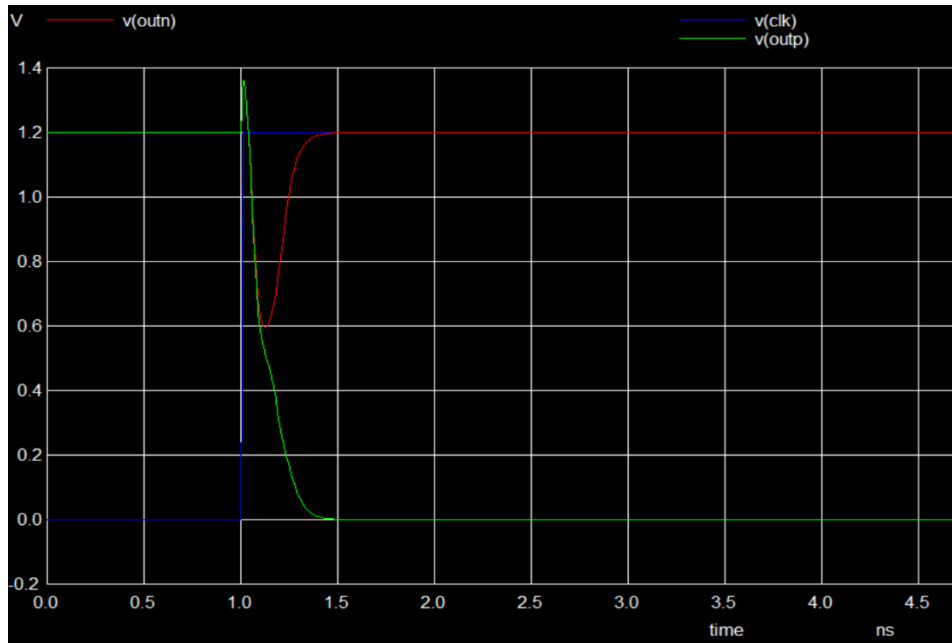
The first stage performs the initial comparison, while the second stage uses positive feedback to regenerate the small voltage difference into full logic levels.

3.3.1 Conventional Dynamic Comparator with Cross-Coupled Latch



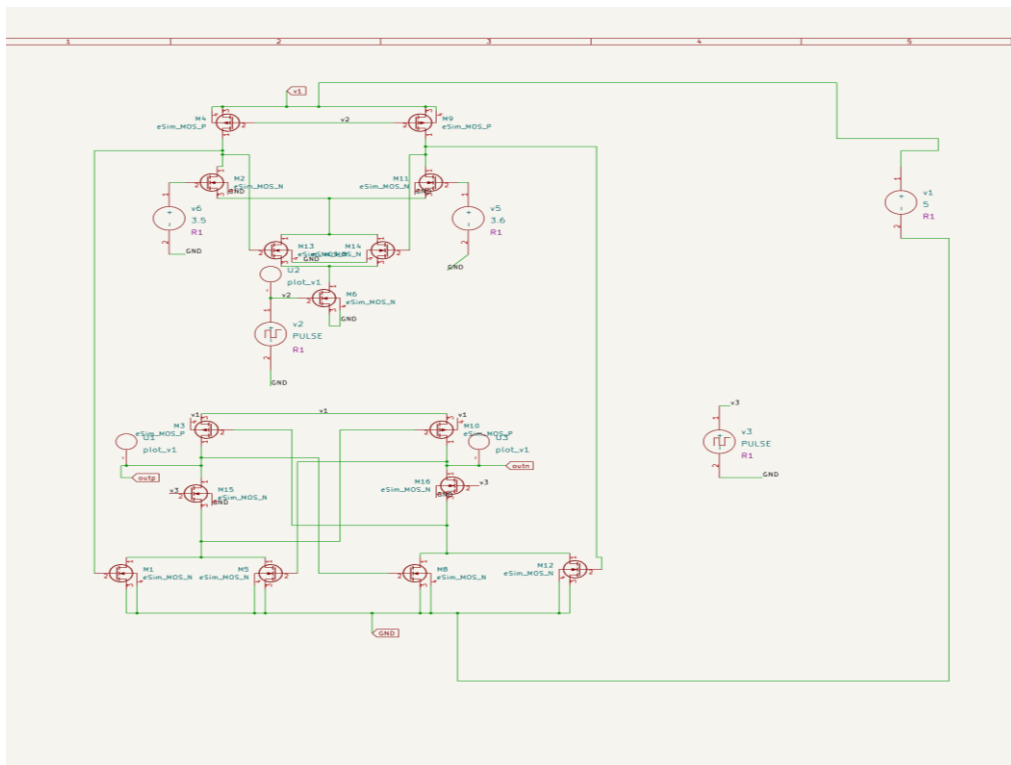
Observations:

- Clear and non-overlapping outputs are observed after the latch activates.
- The outputs resolve much faster compared to the conventional dynamic comparator.
- *The two-stage dynamic comparator with cross-coupled latch demonstrates superior performance compared to the conventional architecture by enabling fast regeneration, rail-to-rail outputs, and improved noise immunity.*



3.3.2 Proposed Cascade Dynamic Comparator with Cross-Coupled Latch

- A cascade dynamic comparator as the first stage.
- A cross-coupled latch as the second stage. The paper concludes that this architecture achieves the lowest power dissipation among all evaluated designs, particularly when the cascade transistor widths are optimally chosen.



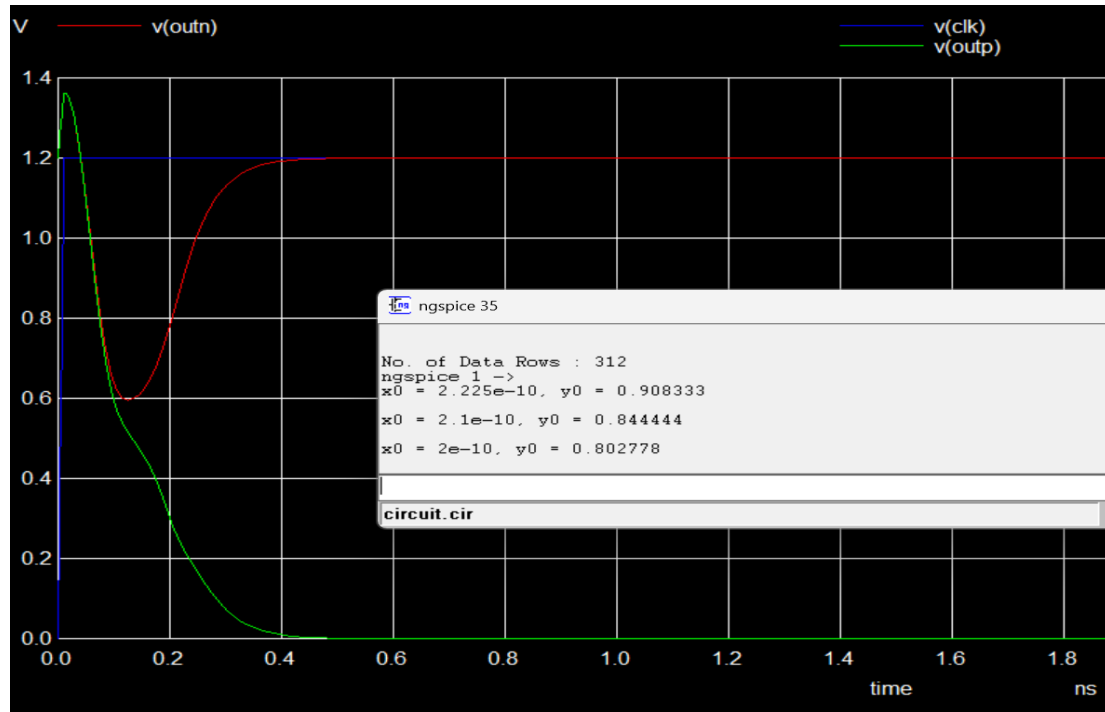


Figure 1: Delay of 200ps very accurate with reference paper readings was observed

4. Outcomes and Analysis

- The expected outcome of this work is a set of working comparator simulations that demonstrate the operational principles described in the research paper.
- The cascade dynamic comparator is expected to show correct clocked operation with low power dissipation, while the two-stage comparator is expected to demonstrate improved decision speed and robustness due to pre-amplification.

EXPECTED values for DELAY (in ps) according to the paper:

Conventional dynamic comparator with cross coupled latch	179.6
Proposed cascade dynamic comparator with cross coupled latch	187.30

ACHIEVED values using eSim:

A delay in the range **190ps-200ps** was observed for the final “*Proposed Cascade Dynamic Comparator with Cross-Coupled Latch circuit*” on **eSim** (ngspice plots).

Although exact numerical matching with the paper’s results is not expected due to differences in technology parameters and models, qualitative trends such as reduced power consumption and improved speed with architectural enhancement should be observable.

Reference Paper Information

- **Title:** *Analysis of Low Power Dynamic Comparator*
- **Authors:** M. Sai Navya, U. Koti Reddy, N. Yaswanth Kumar, G. Sai Krishna, P. Lakshman
- **Journal Name:** *International Journal of Innovative Technology and Exploring Engineering (IJITEE)*
- **Publisher:** Blue Eyes Intelligence Engineering and Sciences Publication
- **Month and Year of Publication:** May 2020
- **Paper Link:** <https://www.ijitee.org/wp-content/uploads/papers/v9i7/G5294059720.pdf>
- **Key Contribution:**
 - Introduction of cascade dynamic comparator and two-stage comparator with cross-coupled latch.
 - Demonstration of reduced dynamic power through transistor sizing optimization, particularly for cascade transistors.

Conclusion

In conclusion, this project analyze low-power dynamic comparator circuits from a published research paper into the eSim environment. By implementing both cascade and two-stage comparator architectures and studying their behavior step by step, increasing design complexity, analytical depth, and research relevance.