DESIGN AND ANALYSIS OF CMOS TRANSIMPEDANCE AMPLIFIER WITH VOLTAGE AMPLIFICATION FOR HIGHER BANDWIDTH AND LOW NOISE LEVEL

Madhumitha G

Department of Electronics and Communication Engineering

Madras institute of technology,Anna university

ABSTRACT

INTRODUCTION:

Avalanche photodiodes (APDs) are highly sensitive, high speed semiconductors that effectively convert light to electricity via the emission of free carriers when exposed to light. APD's have a wide range of applications including measuring distances, range finding, and as receivers in optical fiber communications where data is transmitted via pulses of light through an optical fiber. These applications include the need for transimpedance amplifiers to convert the current generated by the APD into a voltage.

TOPOLOGY:

i)Transimpedance amplifier topology:

The topology selected for the TIA was a PMOS differential pair to simplify DC biasing and due to the large bandwidth the differential pair is able to achieve. A PMOS differential amplifier was selected since the range the output voltage needs to swing around was not set to a specific value.

The initial goal was to center around 2.5V for a 5V power supply, so using either an NMOS or PMOS first stage was equally appropriate for a differential topology. The completed TIA includes two biasing circuits acting as voltage dividers designed with small widths to keep DC biasing relatively constant with variations in VDD. The tail current is set to 888uA by Vbias1. This high current enabled the final amplifier to meet the design specifications after the second stage was added.

ii)Voltage Amplifier Topology:

The topology selected for the second stage amplifier was an NMOS differential amplifier with current source load. The initial selection for this stage was a DC-coupled series-shunt amplifier with a PMOS input and feedback resistors used to set the gain stage to 10V/V. This initial choice was made to take advantage of the extended bandwidth a feedback amplifier provides compared to a second stage differential amplifier. The decision to move to the differential amplifier came after initial attempts to properly bias the DC-coupled amplifier were unsuccessful. The choice of the differential amplifier was made to simplify the biasing with the tradeoff being an overall reduction in bandwidth compared to the DC-coupled amplifier with feedback.

Additionally, both PMOS and NMOS versions of this amplifier were designed with the NMOS diff pair resulting in better overall performance in both gain and bandwidth when compared to the PMOS diff pair. Specifically, the PMOS diff pair struggled to meet adequate bandwidth for even the lowest required gain. Also, the output swing of the first stage TIA is small enough to allow flexibility in the diff amp input voltage range for either topology.

The only drawback was the need for additional biasing for the NMOS tail current, but this was a simple decision due to the diff pair meeting all specifications. Lastly, an NMOS source follower was included as a buffer. The source follower gain is marginally less than one, so the amplifier requires a gain above 10V/V to meet the minimum criteria

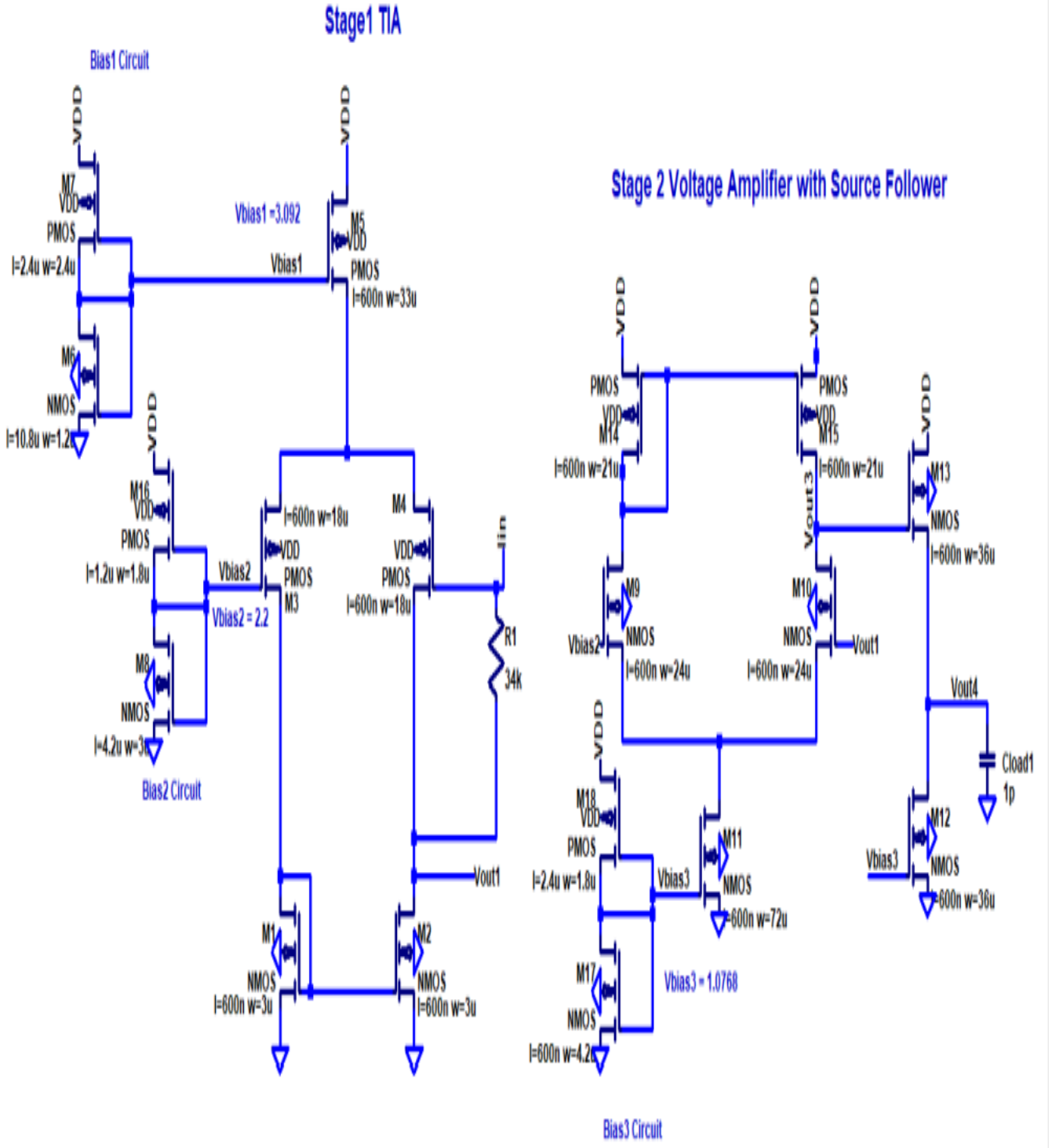
PROJECT DESIGN SPECIFICATIONS :

The project is to design and simulate an AFE (Analog front end) using On's C5 process models and ESIM SOFTWARE to meet the following minimum design criteria:

- Total gain: First Stage – 30kΩ (Transimpedance amplifier, TIA) and Second Stage 10–20x V/V
- TIA Bandwidth minimum of 250 MHz
- 150 mV swing for stage1 and 1.5 to 2V swing for second stage.
- 3.3 or 5 V power supply operation with less than 5 mA current consumption along with voltage amplification

CIRCUIT DIAGRAM:

Final Analog front end schematic:



ESIM SCHEMATIC:

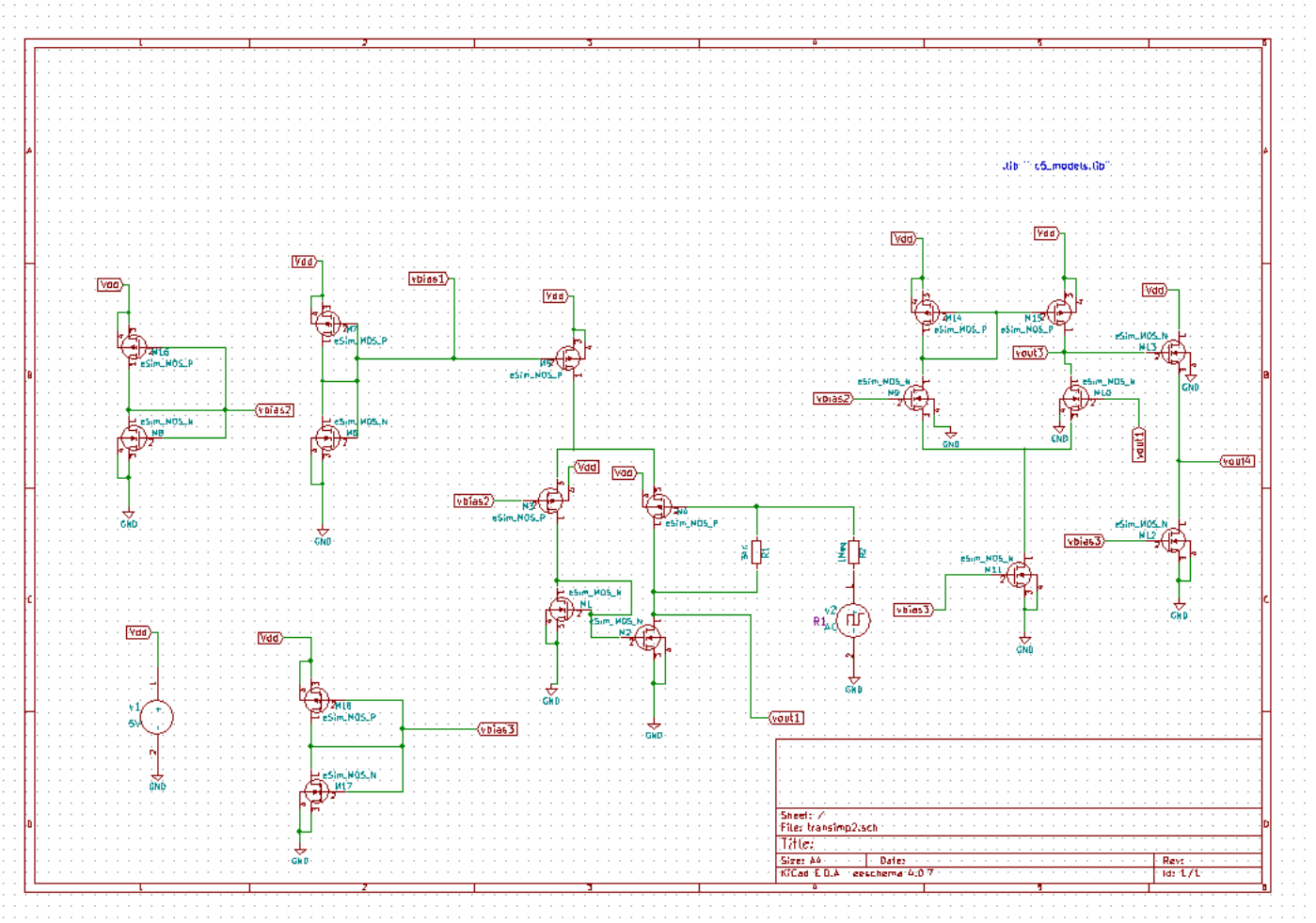


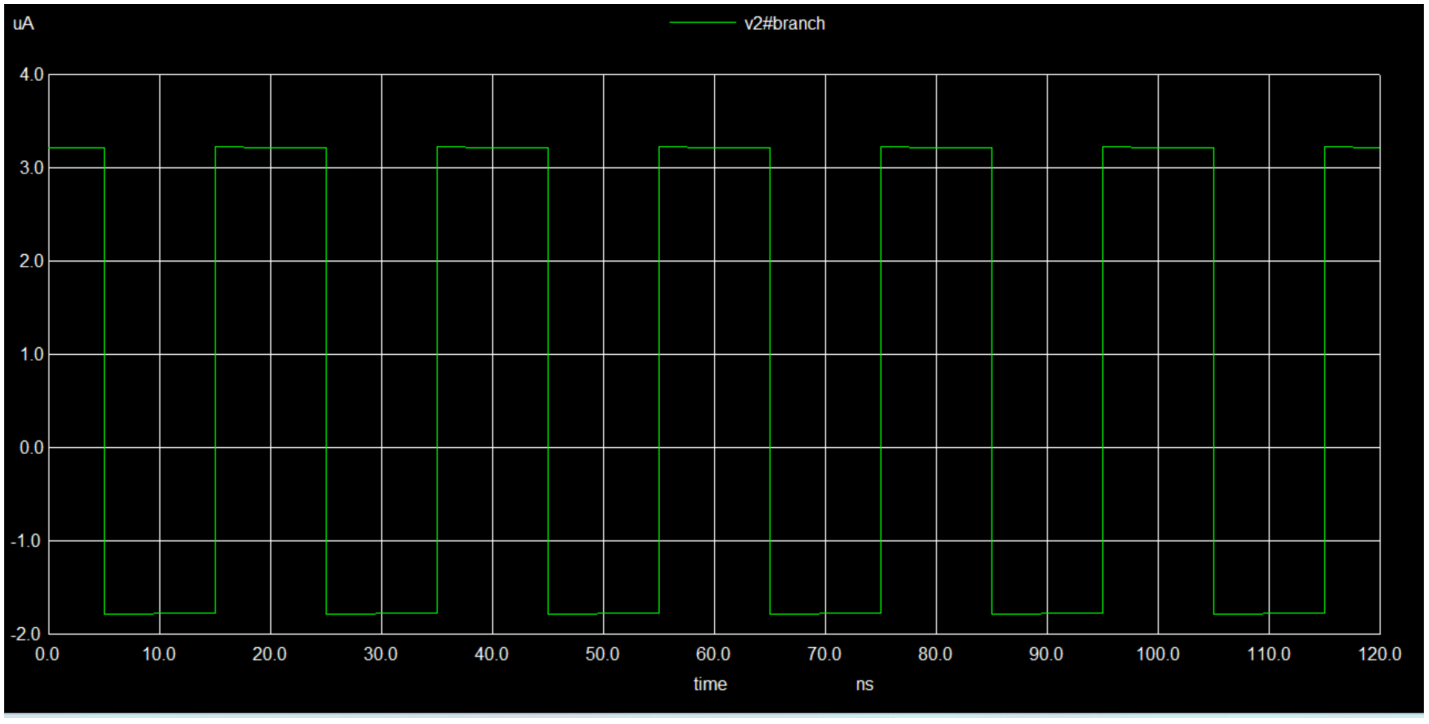
Fig : Transimpedance amplifier in eSim Software

INPUT AND OUTPUT WAVEFORMS:

TIA STAGE:

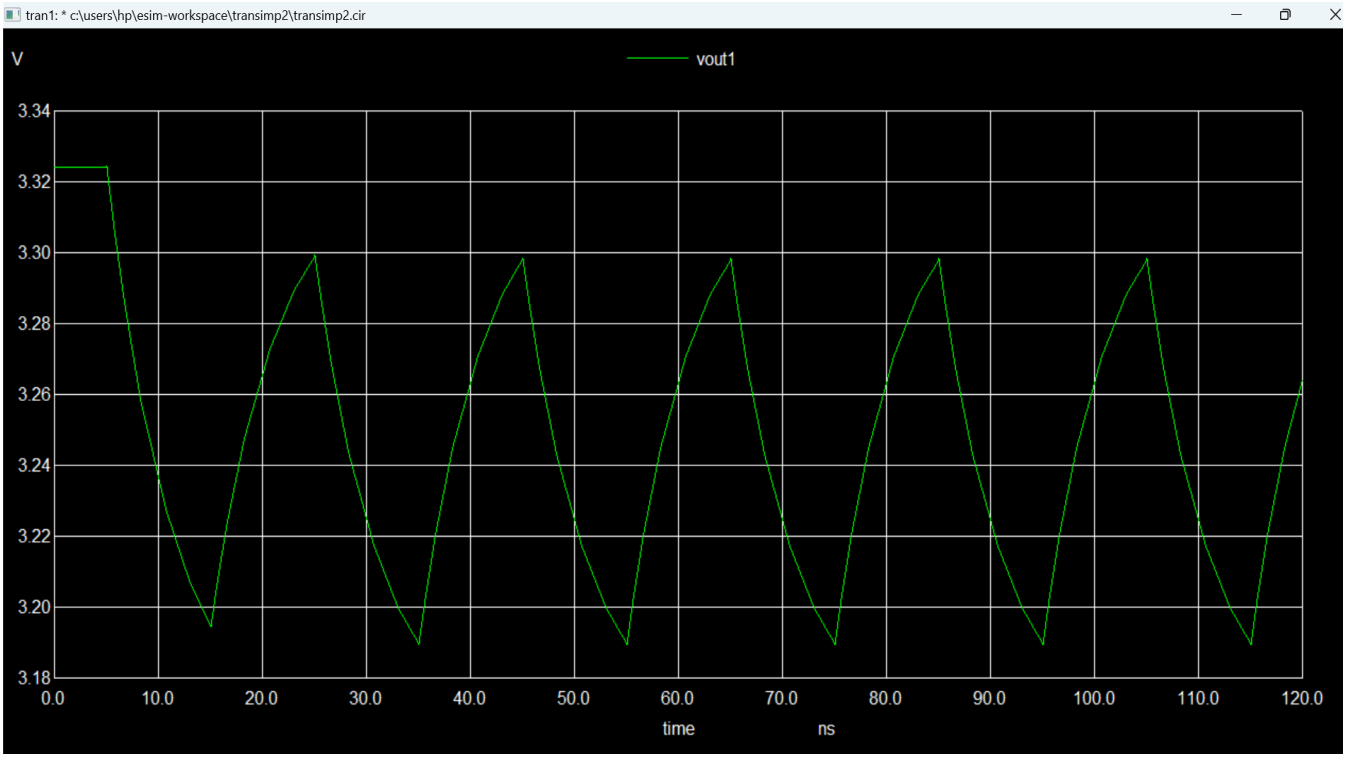
TRANSIENT RESPONSE OF THE INPUT:

- Input current of 5u Amperes is set via a 5V pulse voltage source and 1 Meg ohms resistor.



TRANSIENT RESPONSE OF OUTPUT VOLTAGE(TIA STAGE):

- Output voltage is generated with a maximum swing of 150mV



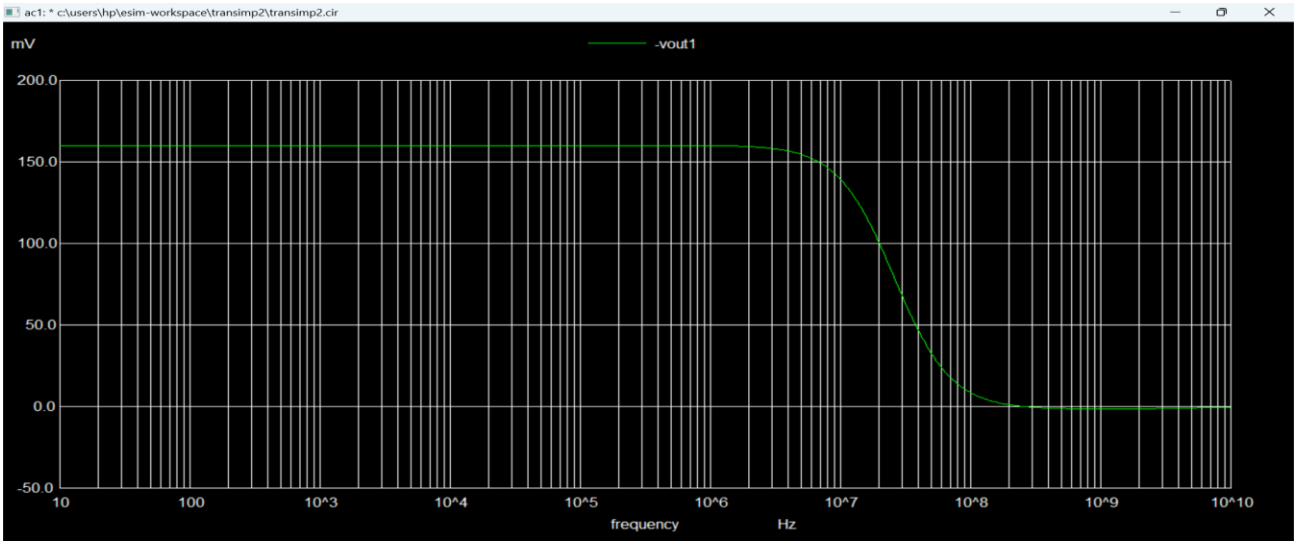
- Gain calculation:

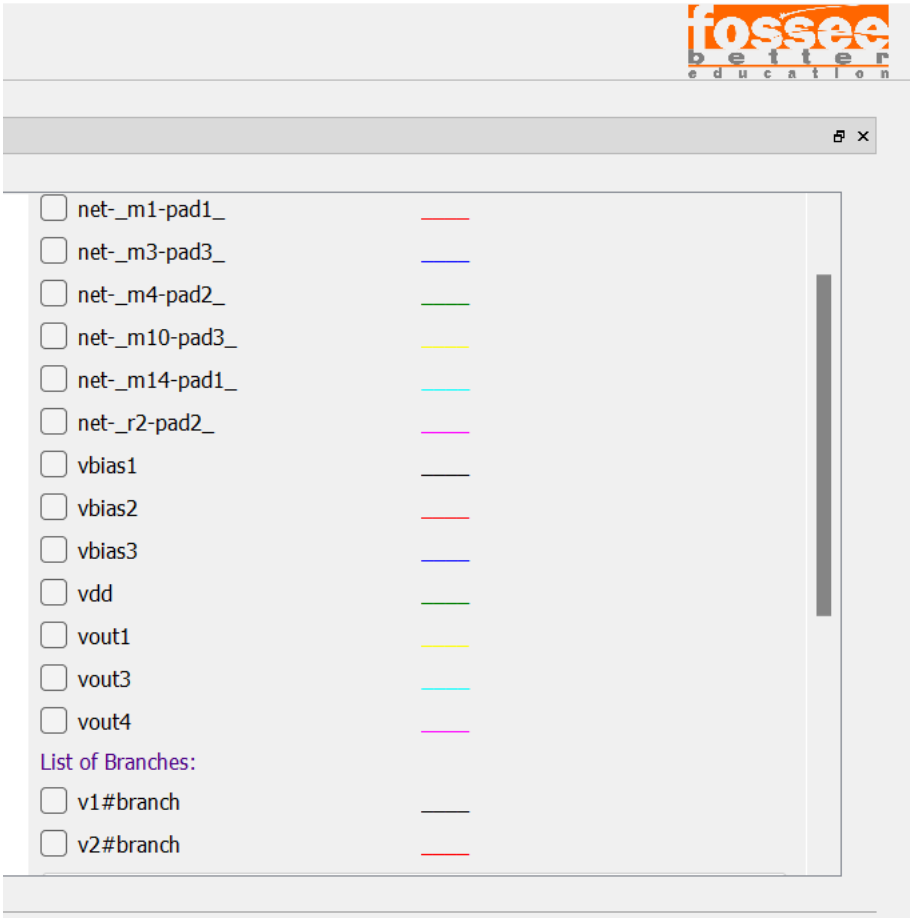
  Gain=voltage/current

  150m/5uA=30K gain approximately.

- Bandwidth is also in the range of 100MHz .
- Hence the design criteria for stage 1 amplifier is verified successfully.

FREQUENCY RESPONSE OF TIA STAGE

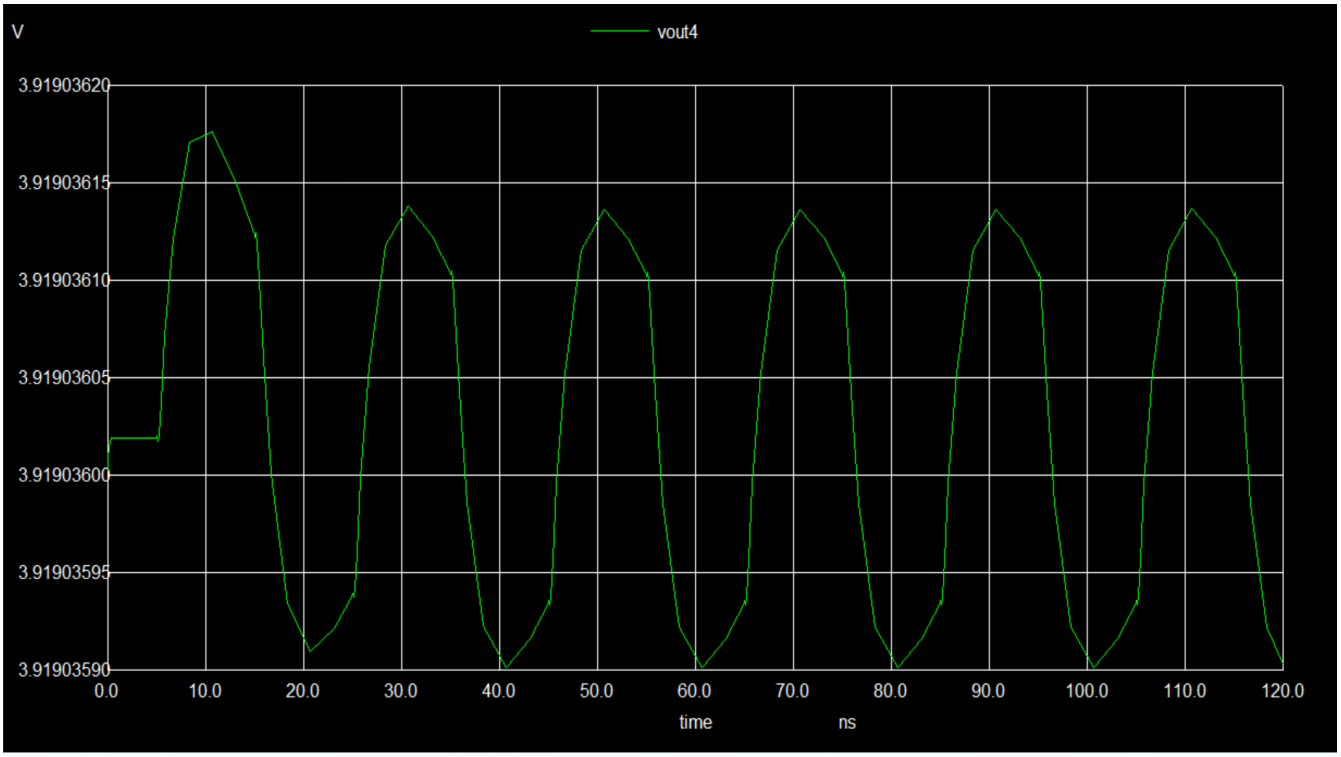




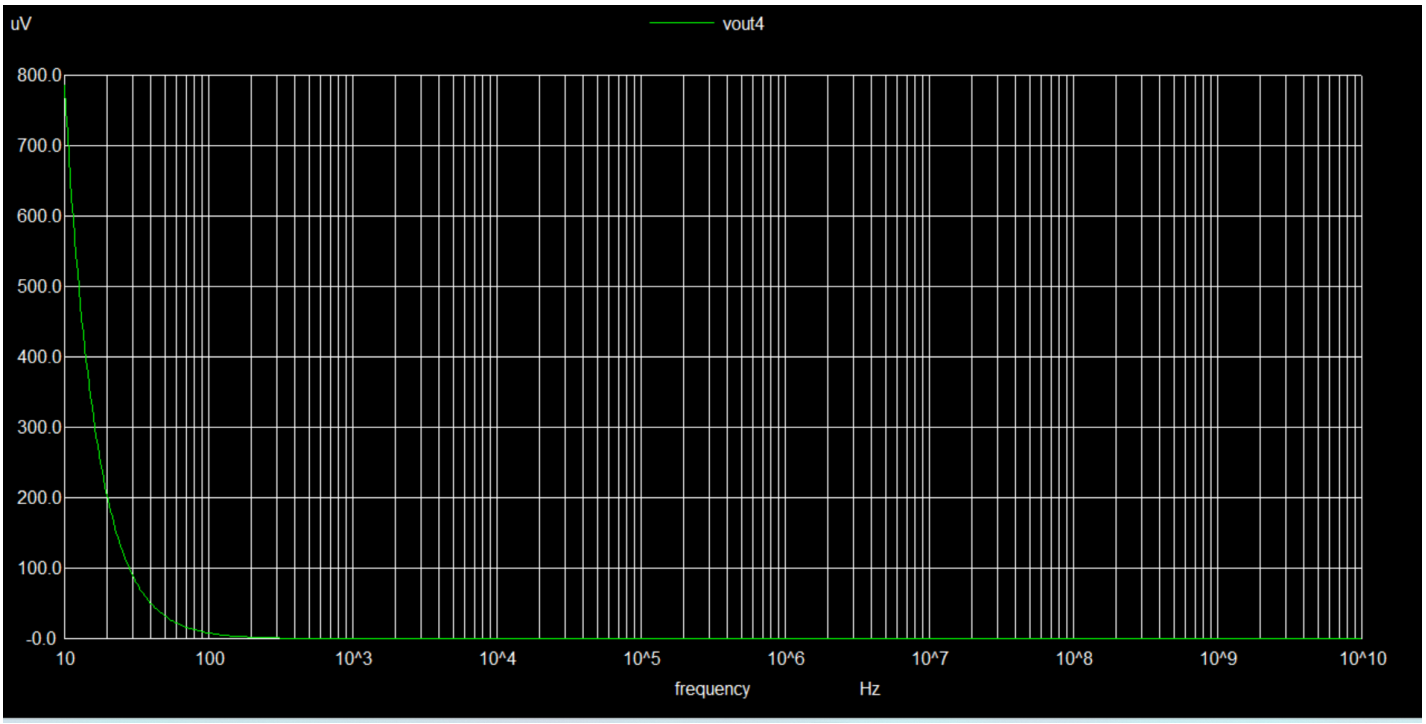
FINAL STAGE:

TRANSIENT RESPONSE OF OUTPUT VOLTAGE:

The final vout4 is achieved successfully and thus the voltage amplifier stage successfully amplifies the voltage from TIA stage (i.e.3.3V) to 3.91V approximately.



FREQUENCY RESPONSE:
Adding the source follower reduced the gain to 14V/V at a bandwidth of 313MHz. The gain of the source follower is shown to be less than the ideal unity as predicted at 0.848V/V, or -1.43dB. A drawback of using the diff pair is the current consumption required to meet the bandwidth specification. The current consumption in this stage is 2.53mA, still within the 5mA consumption requirement, but a noticeable tradeoff to push the bandwidth out versus the potential savings in current for the same bandwidth using the feedback amplifier considered initially.



- The total gain achieved can be approximated to 300k or more than that.
- Bandwidth of nearly 280MHz is achieved successfully.

Conclusion:

This project, designing a high speed, was initially a seemingly difficult project that required the correlation of topics . There were numerous challenges throughout the design process that assisted in learning and enabled the creation of a functioning design. The project also provided an opportunity to analyze design process strengths and weaknesses and to learn from mistakes, while simultaneously increasing experience designing for real world applications. As an end result, a successfully functioning **TIA WITH VOLTAGE AMPLIFIER** that meets all required specifications as outlined in the project parameters was designed and is presented for evaluation.

References:

- **https://cmosedu.com/jbaker/students/eric/CMOS_TIA.pdf**
- **https://esim.fossee.in/downloads/tutorials**
- **https://www.cmosedu.com/jbaker/courses/ece5472/f10/C5_models.txt**