Design and Power Analysis of a 2-Bit Magnitude Comparator Using GDI and CMOS Techniques in eSim

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Abstract

Magnitude comparators are fundamental building blocks in digital systems, widely used in arithmetic logic units, control circuits, and data comparison applications. As VLSI technology scales, power consumption and transistor count become critical design constraints.

This project presents the design and simulation of a 2-bit magnitude comparator using CMOS and Gate Diffusion Input (GDI) logic techniques. The circuit is implemented and verified using the open-source eSim (ngspice) simulation platform developed under the FOSSEE initiative. The proposed design focuses on correct logical operation, reduced complexity, and power-efficient implementation. Simulation results validate the functionality of the comparator for all possible input combinations, demonstrating the suitability of eSim for educational and research-oriented VLSI design.

Keywords: Magnitude Comparator, CMOS Logic, GDI Technique, eSim, ngspice, Low Power VLSI

Contents

1 Introduction

Comparison operations form the backbone of decision-making in digital systems. From arithmetic processing to control flow and data sorting, magnitude comparators are indispensable components of modern digital hardware.

A magnitude comparator compares two binary numbers and generates outputs indicating whether one number is greater than, equal to, or less than the other. While simple in concept, comparator design becomes challenging in VLSI systems due to increasing power constraints, area limitations, and performance requirements.

Conventional CMOS logic offers reliable operation but requires a large number of transistors, leading to increased power dissipation. Gate Diffusion Input (GDI) logic has emerged as an effective alternative, enabling complex logic functions with fewer transistors and lower power consumption.

This project aims to design and analyze a 2-bit magnitude comparator using CMOS and GDI techniques, simulated using the eSim tool based on ngspice.

2 Objective

The main objectives of this project are:

- To design a 2-bit magnitude comparator using conventional CMOS logic.
- To design an optimized 2-bit magnitude comparator using Gate Diffusion Input (GDI) technique.
- To implement both CMOS and GDI based designs at the transistor level.
- To simulate and verify the functional correctness of both designs using eSim (ngspice).
- To analyze and compare the power consumption of CMOS and GDI implementations.
- To evaluate the effectiveness of GDI logic in reducing transistor count and power dissipation.

3 Problem Statement

Traditional CMOS-based comparator circuits suffer from high transistor count and increased power consumption, which limits their applicability in low-power systems. As portable and embedded devices demand energy-efficient hardware, there is a need for compact comparator designs with reduced power dissipation.

The problem addressed in this work is the design of a 2-bit magnitude comparator that ensures correct functionality while minimizing circuit complexity and power consumption using CMOS and GDI logic techniques.

4 Theory of 2-Bit Magnitude Comparator

Let the two 2-bit binary numbers be:

$$A = A_1A_0, \quad B = B_1B_0$$

The comparator generates three outputs:

- $A > B$
- $A = B$
- $A < B$

The comparison starts from the most significant bit. Logical expressions for the outputs are derived as:

$$A = B = (A_1 \odot B_1)(A_0 \odot B_0)$$

$$A > B = A_1B_1' + (A_1 \odot B_1)A_0B_0'$$

$$A < B = A_1'B_1 + (A_1 \odot B_1)A_0'B_0$$

where $\odot$ represents the XNOR operation.

5 Design Methodology

The comparator is designed as a combinational circuit and implemented at the transistor level using two approaches: CMOS and GDI (Gate Diffusion Input). In the CMOS implementation, basic logic gates (AND, OR, NOT, XOR/XNOR) are constructed using complementary NMOS and PMOS transistors, ensuring stable operation. In the GDI implementation, the same logic functions are realized with fewer transistors, optimizing for area and power while maintaining correct logic functionality. Complementary signals required for the circuits are generated using CMOS inverters. Both designs are simulated separately in eSim to verify logic correctness, voltage levels, power consumption, and propagation delay, enabling a comparative analysis between CMOS and GDI implementations.

6 Simulation Setup Using eSim

Transient analysis is performed using ngspice. Pulse voltage sources are applied to inputs to cover all possible combinations. Output waveforms are observed to validate logical correctness.

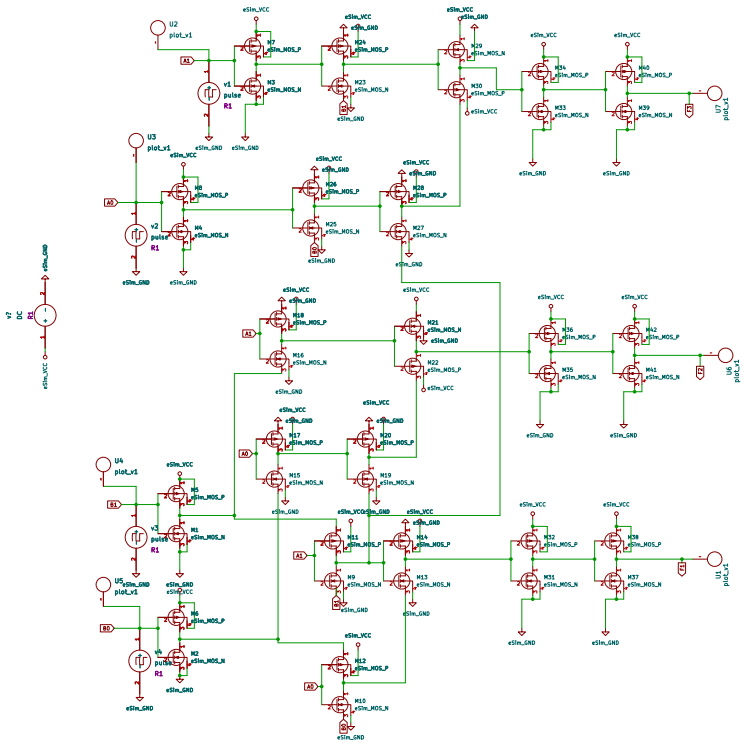

Figure 1: Schematic of Magnitude Comparator using GDI Technique

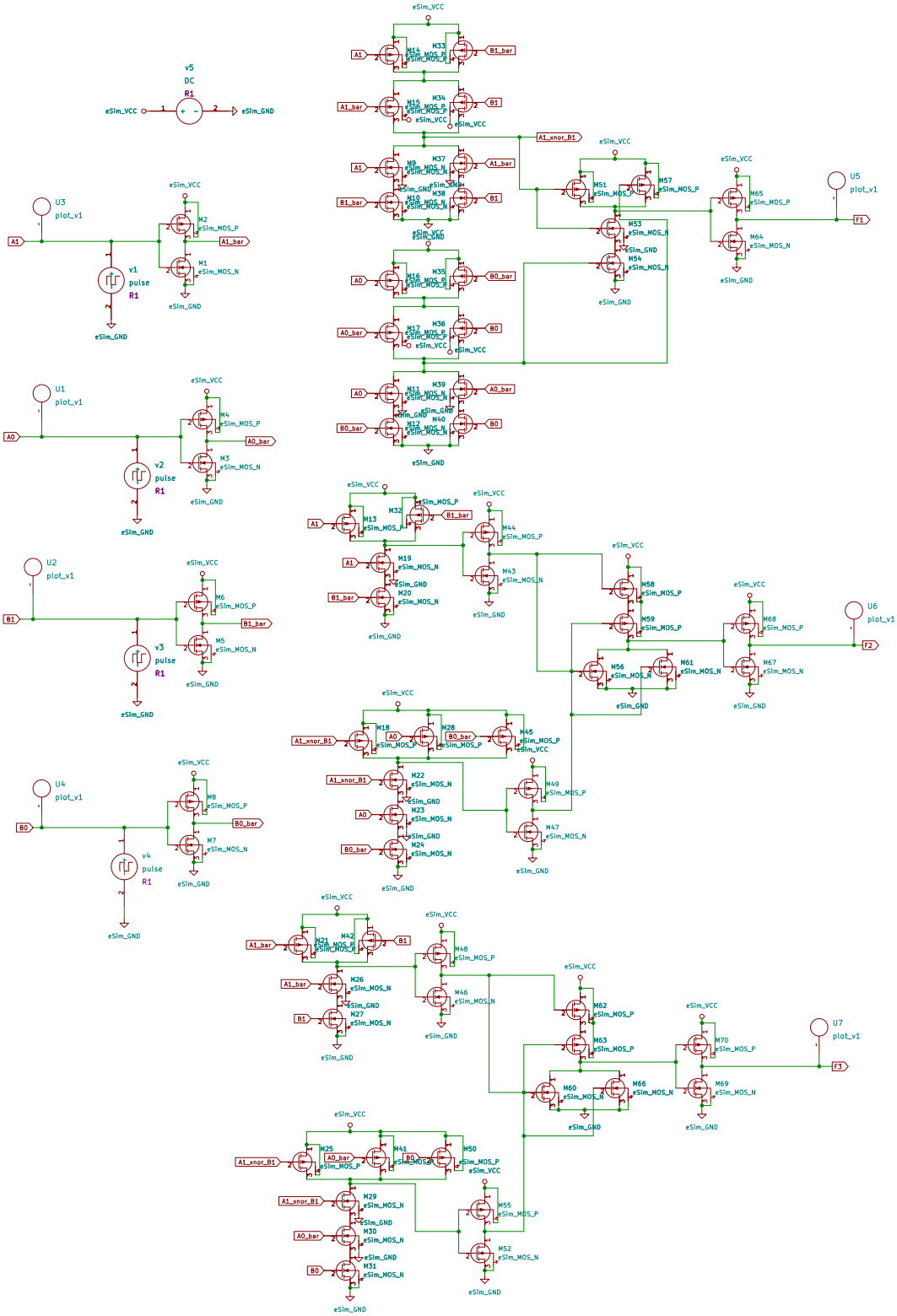

Figure 2: Schematic of Magnitude Comparator using CMOS Technology

Note: $f_1 = (a = b),\ f_2 = (a > b),\ f_3 = (a < b)$

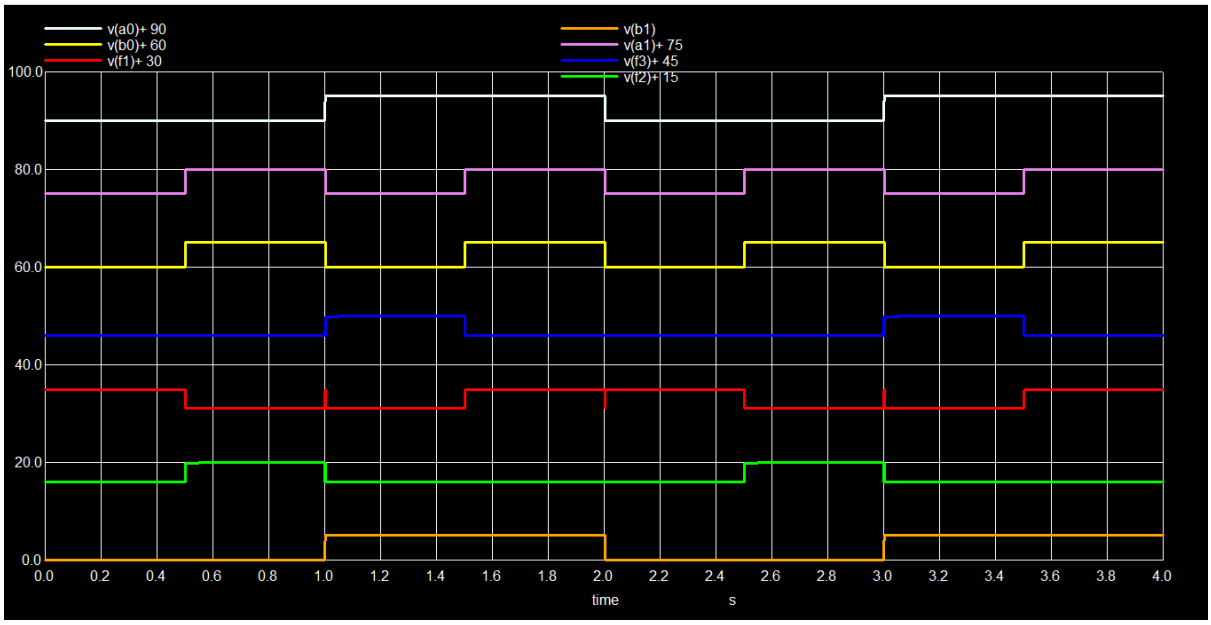

Figure 3: Simulation of Magnitude Comparator using GDI Technique

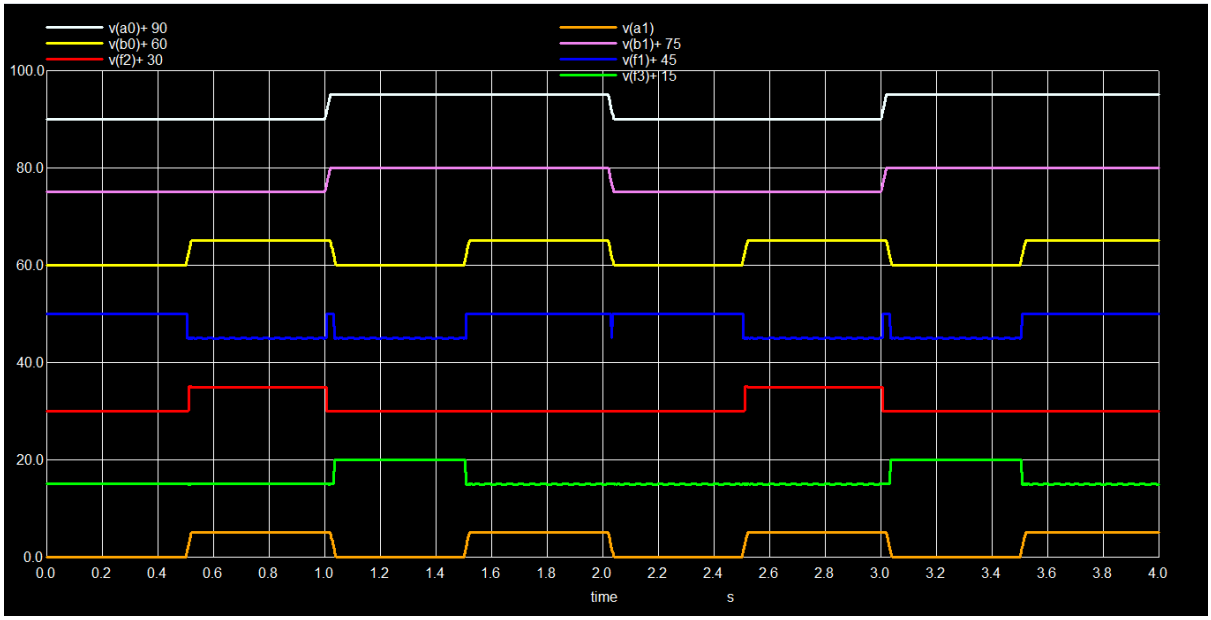

Figure 4: Simulation of Magnitude Comparator using CMOS Technology

7 Results and Discussion

The simulation results confirm correct operation of the 2-bit magnitude comparator for all input combinations. The outputs accurately indicate greater than, equal to, and less than conditions.

The use of GDI logic reduces transistor count and contributes to lower power dissipation compared to conventional CMOS-only designs. This demonstrates the effectiveness of power-aware logic techniques in VLSI design.

Truth Table of 2-Bit Magnitude Comparator

A1	A0	B1	B0	A > B	A = B	A < B
0	0	0	0	0	1	0
0	0	0	1	0	0	1
0	0	1	0	0	0	1
0	0	1	1	0	0	1
0	1	0	0	1	0	0
0	1	0	1	0	1	0
0	1	1	0	0	0	1
0	1	1	1	0	0	1
1	0	0	0	1	0	0
1	0	0	1	1	0	0
1	0	1	0	0	1	0
1	0	1	1	0	0	1
1	1	0	0	1	0	0
1	1	0	1	1	0	0
1	1	1	0	1	0	0
1	1	1	1	0	1	0

Figure 5: Truth Table of the Comparator Circuit

Comparator Type	No. of Transistors	Power	Area	Technology
CMOS	70	2.54mW	more	180nm
GDI	42	40 µW	less	180nm

Figure 6: Performance Comparison of CMOS and GDI Comparator Circuits

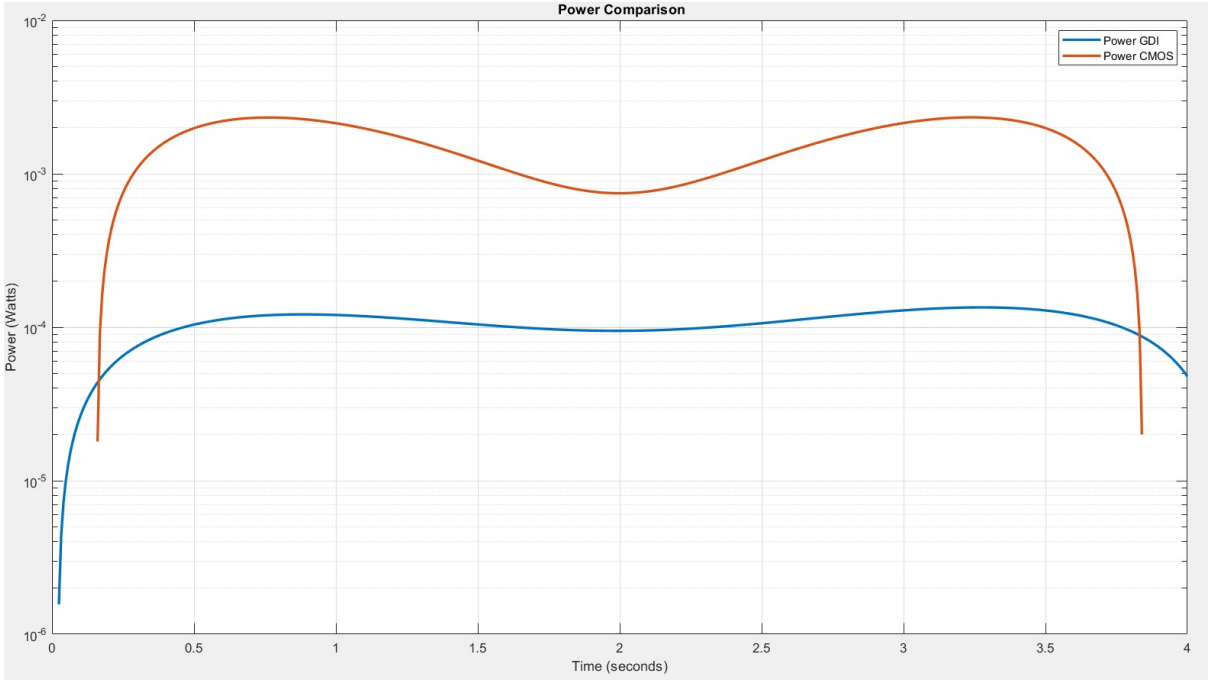

Figure 7: Power Consumption Comparison of CMOS and GDI Comparators

8 Applications

- Arithmetic Logic Units (ALUs)
- Digital signal processing systems
- Sorting and comparison hardware
- Microprocessors and controllers
- Decision-making circuits

9 Conclusion

A 2-bit magnitude comparator was designed and simulated using CMOS and GDI logic in eSim. Correct functionality was verified, and power analysis showed that the GDI implementation consumes significantly less power than CMOS. The project demonstrates the suitability of GDI logic for low-power VLSI design and the effectiveness of eSim as an open-source EDA tool under the FOSSEE initiative.

10 References

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