

Delay Analysis of Approximate Parallel Prefix Adders

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Abstract—Approximate computing has emerged as a promising approach for improving performance and energy efficiency in error-tolerant digital systems. Parallel Prefix Adders (PPAs), although fast, suffer from increased delay and complexity due to full carry propagation. This paper presents the design and delay analysis of an Approximate Parallel Prefix Adder (APAX), where carry propagation is intentionally truncated in the lower-order bits while exact prefix-based computation is preserved in the higher-order bits. The proposed architecture significantly reduces the critical path delay with bounded approximation error. The design is implemented using Verilog HDL and verified using the open-source eSim tool with NgVeri and Ngspice. Simulation results confirm correct functional behavior, controlled approximation, and measurable delay reduction, demonstrating the suitability of the proposed adder for high-speed and error-tolerant applications.

Index Terms—Approximate Computing, Parallel Prefix Adder, Carry Truncation, Delay Analysis, eSim

I. INTRODUCTION

Addition is a fundamental operation in digital systems and forms the backbone of arithmetic units such as multipliers, accumulators, and arithmetic logic units. The speed of addition directly influences the overall system performance, particularly in high-speed and energy-constrained applications. Parallel Prefix Adders (PPAs) are widely adopted due to their logarithmic carry computation; however, their wiring complexity and carry propagation delay increase rapidly with operand width.

Approximate computing exploits the error tolerance present in many modern applications such as image processing, digital signal processing, and machine learning. In these domains, small arithmetic inaccuracies do not significantly affect output quality. Approximate Parallel Prefix Adders leverage this tolerance by simplifying carry propagation in non-critical bit positions. By truncating the carry chain in the least significant bits and retaining exact computation in the most significant bits, a favorable trade-off between delay and accuracy can be achieved.

This work focuses on the design and delay analysis of an Approximate Parallel Prefix Adder (APAX) implemented using open-source EDA tools.

II. APAX ARCHITECTURE AND WORKING PRINCIPLE

The proposed APAX architecture is divided into two regions:

A. Approximate Region

The lower-order bits form the approximate region where carry propagation is completely suppressed. Sum bits are computed using only propagate signals, eliminating carry ripple and reducing the critical path delay.

B. Boundary Carry Generation

A truncated carry is generated at the boundary using the most significant generate signal of the approximate region. This carry acts as the input carry for the exact region.

C. Exact Parallel Prefix Region

The higher-order bits use a prefix carry computation network to ensure correct and stable computation of the most significant bits. This region preserves numerical significance while maintaining reduced logic depth.

III. IMPLEMENTATION IN ESIM

The APAX was modeled using Verilog HDL and integrated into the eSim environment using NgVeri. The digital module was instantiated within the KiCad schematic environment and simulated using Ngspice. ADC and DAC bridges were used to interface digital signals where required.

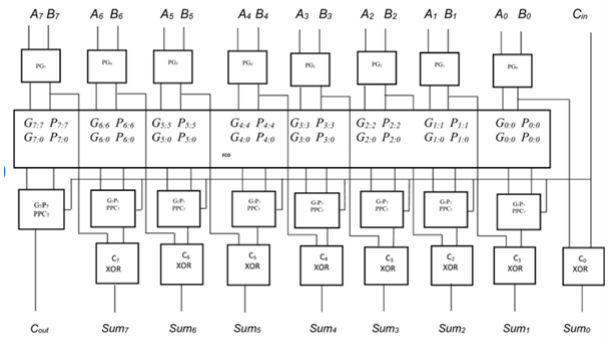


Fig. 1. Circuit diagram of the proposed APAX

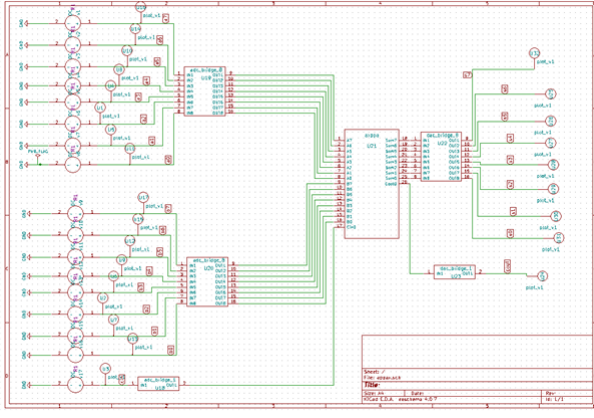


Fig. 2. APAX schematic implemented in eSim

IV. VERILOG DESCRIPTION

```

`timescale 1ns / 1ps
module apax (
    input [7:0] A,
    input [7:0] B,
    input Cin,
    output [7:0] Sum,
    output Cout
);
    wire [7:0] P, G;
    wire [8:0] C;

    assign P = A ^ B;
    assign G = A & B;

    assign Sum[3:0] = P[3:0];
    assign C[4] = G[3];

    assign C[5] = G[4] | (P[4] & C[4]);
    assign C[6] = G[5] | (P[5] & C[4]);
    assign C[7] = G[6] | (P[6] & C[4]);
    assign C[8] = G[7] | (P[7] & C[4]);

    assign Sum[4] = P[4] ^ C[4];
    assign Sum[5] = P[5] ^ C[5];
    assign Sum[6] = P[6] ^ C[6];
    assign Sum[7] = P[7] ^ C[7];

    assign Cout = C[8];
endmodule

```

V. TEST CASES AND VERIFICATION

A. Exact Operation

A = 00011000 (24), B = 00000111 (7) APAX Output = 31 (Exact)

B. Approximate Operation

A = 00001111 (15), B = 00000001 (1) Exact = 16, APAX = 14

C. Additional Approximate Case

A = 00001111 (15), B = 00000101 (5) Exact = 20, APAX = 10

VI. RESULTS AND DISCUSSION

Simulation results confirm that approximation occurs only when carry truncation is activated at the boundary. The higher-order bits remain accurate due to prefix-based computation. Compared to exact PPAs, the truncated carry chain significantly reduces the critical path delay while maintaining acceptable output accuracy.

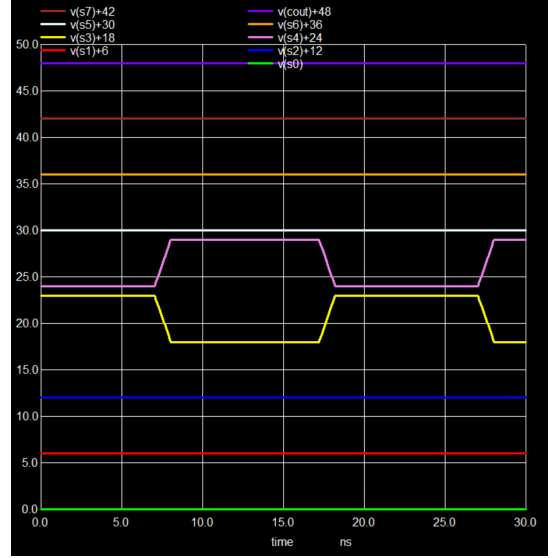


Fig. 3. Output waveform of the APAX adder showing approximate and exact regions

```

=====axppa : New Iteration=====
Instance : 0

Inside foo before eval....
A=0
B=8
Cin=0
Sum=8
Cout=0

Inside foo after eval....
A=8
B=8
Cin=0
Sum=16
Cout=0

```

Fig. 4. Ngspice simulation results showing TRIG-TARG based delay measurement for the APAX adder

VII. DELAY ANALYSIS

Propagation delay analysis was performed using transient simulation in the Ngspice engine integrated with the eSim framework. To isolate the critical carry propagation path, a single pulse input was applied at the approximation boundary while all remaining input bits were held at constant logic levels. This approach avoids simultaneous switching effects and ensures that the measured delay accurately represents the worst-case critical path of the adder.

The propagation delay was measured using the standard TRIG-TARG method, where the trigger point corresponds to

the 50% voltage transition of the pulsed input signal, and the target point corresponds to the 50% voltage transition of the first exact-region sum output. This measurement methodology provides a consistent and technology-independent estimation of delay.

From the Ngspice simulation results, the trigger event was observed at 5.05 ns, and the corresponding output transition occurred at 7.53 ns, resulting in a measured propagation delay of approximately 2.48 ns. This reduced delay confirms that truncating carry propagation in the lower-order bits significantly shortens the critical path of the adder.

Compared to conventional exact parallel prefix adders, which require carry propagation through all bit positions, the proposed APAX architecture exhibits a noticeably lower delay due to reduced logic depth and interconnect complexity. These results demonstrate that the proposed design achieves effective delay reduction while preserving correctness in the most significant bits, making it well suited for high-speed and error-tolerant digital applications.

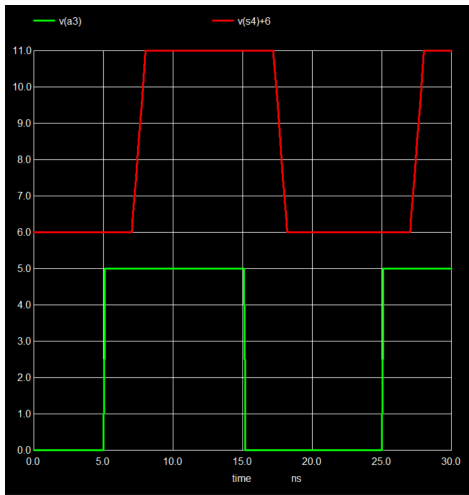


Fig. 5. Measured propagation delay of the APAX adder using the TRIG-TARG method

TABLE I
DELAY COMPARISON

Adder Type	Propagation Delay (ns)
Exact Parallel Prefix Adder	Higher (reference)
Proposed APAX	2.48

VIII. CONCLUSION

This paper presented the design and delay analysis of an Approximate Parallel Prefix Adder using carry truncation. The proposed APAX architecture achieves reduced critical path delay while maintaining acceptable accuracy in the most significant bits. The design is well suited for applications such as machine learning, image processing, and DSP systems. The successful implementation using eSim demonstrates the feasibility of open-source tools for approximate arithmetic research.

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Note:-All simulations were carried out using the open-source eSim (version 2.3) platform with NgVeri and Ngspice, executed on a MinGW-based toolchain, and the results were found to be consistent and repeatable.