Cross charge control flip flop

Pandiyarajan S,
Dept of Electronics and Communication Engineering,
Chennai Institute of Technology-600069

Abstract

An implicit pulse flip-flop architecture, namely the Cross Charge Control Flip-Flop (XCFF), is proposed to achieve low-power operation in high-speed sequential circuits. The XCFF generates a pulse implicitly based on input data activity, allowing the storage elements to capture clock transitions efficiently. Power consumption is minimized by dividing the dynamic node into two independent nodes, each driven by separate pull-up and pull-down transistors. This structure ensures that only one dynamic node switches during a single clock cycle, significantly reducing unnecessary switching activity without increasing latency. Additionally, the XCFF exhibits a relatively low clock driving load, making it suitable for power-sensitive designs. However, the circuit suffers from unwanted precharge at internal nodes X1 and X2 when processing long sequences of logic '1' and '0', respectively. Furthermore, the conditional shutoff mechanism introduces increased hold time during the rising edge of the clock, particularly when the input data remains low and charge sharing occurs at node X1. These limitations highlight the need for further optimization to improve robustness while maintaining low power consumption..

I. INTRODUCTION

Flip-flops are fundamental storage elements in synchronous digital systems and play a critical role in determining the overall power consumption, speed, and reliability of modern VLSI designs. With aggressive technology scaling and increasing clock frequencies, clock distribution networks and flip-flop circuits contribute a significant portion of total chip power. Therefore, designing energy-efficient flip-flops with reduced clock loading and minimized switching activity has become an important research focus.

Pulse-triggered flip-flops (PFFs) have emerged as an attractive alternative to conventional master–slave flip-flops due to their smaller transistor count, lower clock load, and higher performance. Among PFFs, **implicit pulse-triggered flip-flops** are particularly advantageous because they generate the clock pulse internally, eliminating the need for explicit pulse generator circuits and reducing power dissipation..

The **Cross Charge Control Flip-Flop (XCFF)** is an implicit pulse flip-flop architecture designed to achieve low power consumption while maintaining high operating speed. The key idea of XCFF is the division of a single dynamic node into two distinct dynamic nodes that independently control the pull-up and pull-down paths of the output stage. By doing so, switching activity is limited to only one dynamic node during a clock cycle, depending on the input data transition. This cross-charge control mechanism effectively reduces unnecessary internal node transitions and lowers dynamic power dissipation.

Additionally, XCFF features a reduced clock driving load, making it suitable for low-power and high-frequency applications. The internal pulse generation mechanism enables efficient data capture with minimal latency, while the separation of charge paths improves energy efficiency compared to conventional implicit pulse flip-flops

However, despite its advantages, the XCFF architecture exhibits certain limitations, such as unwanted precharge at internal dynamic nodes under specific data patterns and increased hold time due to charge sharing effects during clock transitions. These challenges motivate further research and optimization to enhance the robustness and performance of XCFF-based designs.

Problem Statement

In modern VLSI systems, flip-flops account for a significant portion of total power consumption due to high clock switching activity and large clock loading. Conventional master–slave flip-flops and even many pulse-triggered flip-flop architectures suffer from excessive dynamic power dissipation caused by unnecessary internal node transitions, redundant precharge operations, and charge sharing effects. These issues become more severe at higher clock frequencies and with advanced technology scaling..

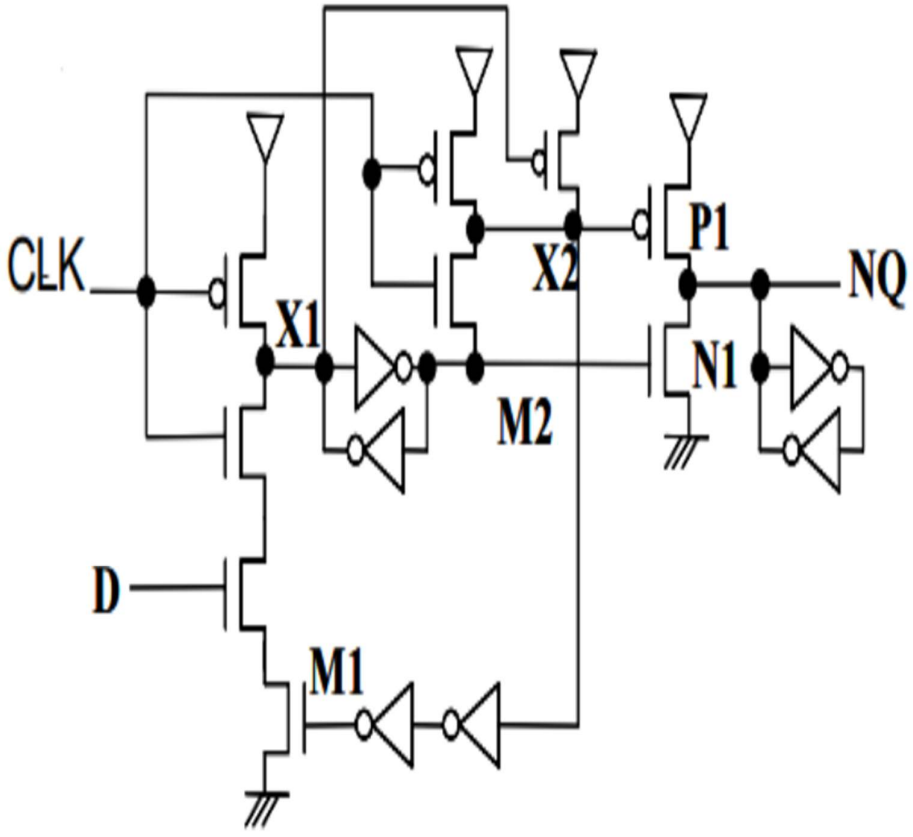
Although the Cross Charge Control Flip-Flop (XCFF) was introduced to reduce power consumption by splitting the dynamic node into two independently driven nodes and minimizing clock-driven switching activity, it still exhibits critical limitations. Unwanted precharge at internal nodes (X1 and X2) occurs under certain data patterns with consecutive logic ‘1’s or ‘0’s, leading to unnecessary power loss. Furthermore, the conditional shutoff mechanism introduces increased hold time during clock transitions due to charge sharing at internal dynamic nodes, which degrades timing robustness and may cause functional errors.

Working Principle

The Cross Charge Control Flip-Flop (XCFF) is an implicit pulse-triggered flip-flop designed to reduce power consumption in high-speed VLSI systems. Unlike conventional flip-flops that rely on a single dynamic node, XCFF divides the dynamic operation into two separate nodes, X1 and X2, which independently control the pull-up and pull-down paths of the output stage. This structure reduces unnecessary internal node switching and lowers the clock driving load

During the clock transition, an implicit pulse is generated internally, allowing the flip-flop to capture input data. Depending on the data value, only one of the dynamic nodes is activated in a clock cycle, while the other remains inactive. This selective charge transfer mechanism significantly reduces dynamic power dissipation without affecting performance, making XCFF suitable for low-power and high-speed applications..

CIRCUIT DIAGRAM



a

eSim Circuit

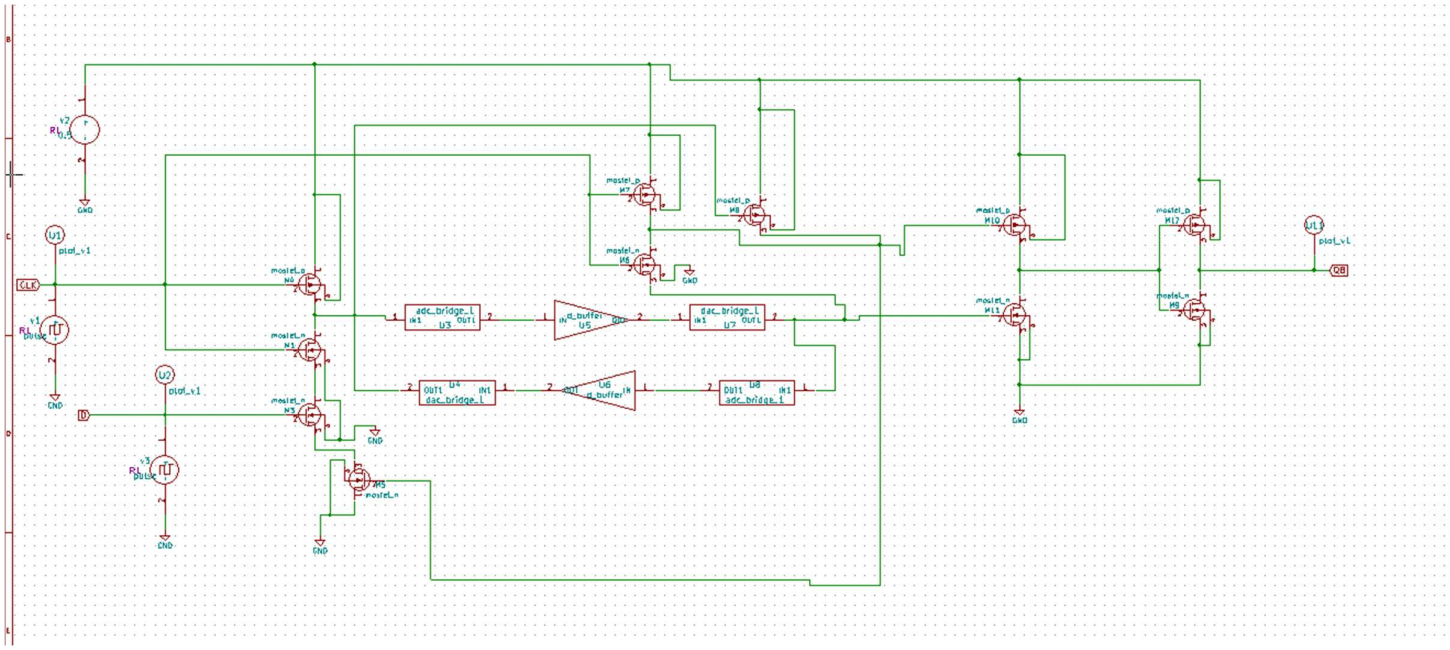
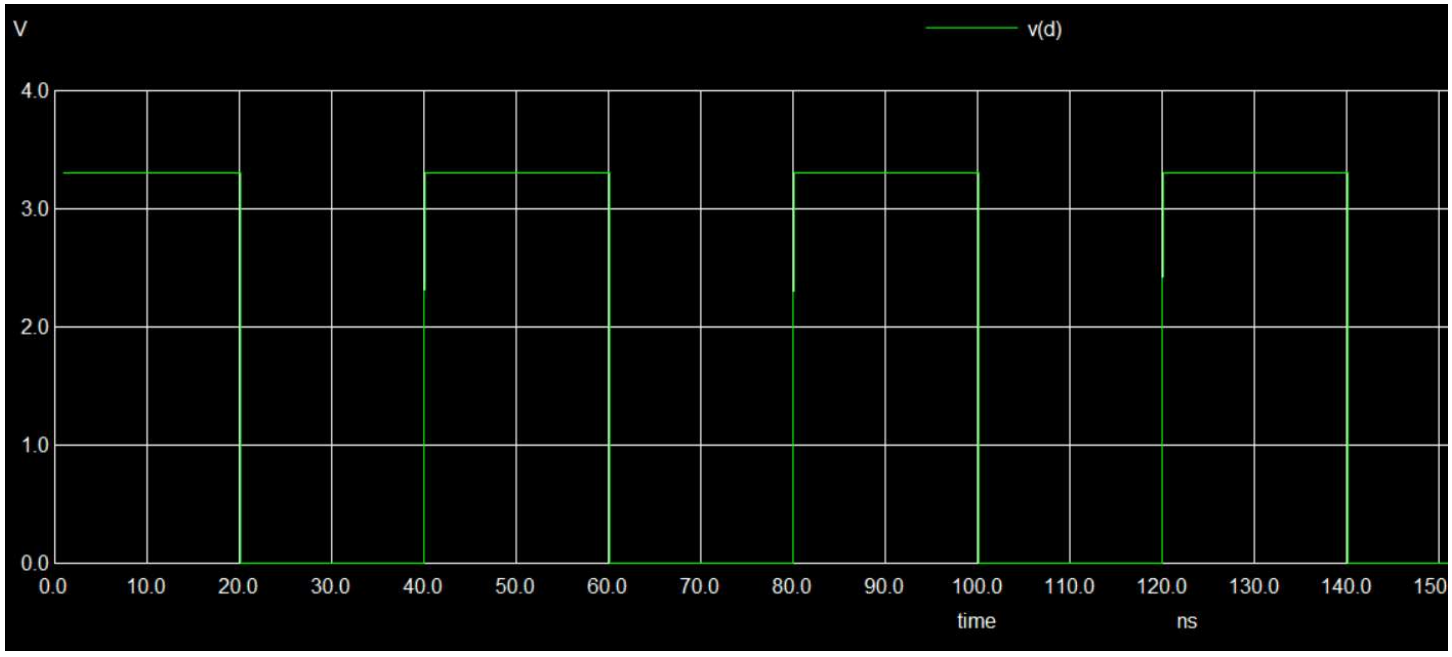


Fig: Circuit Diagram of cross charge control flip flop

INPUT WAVEFORM



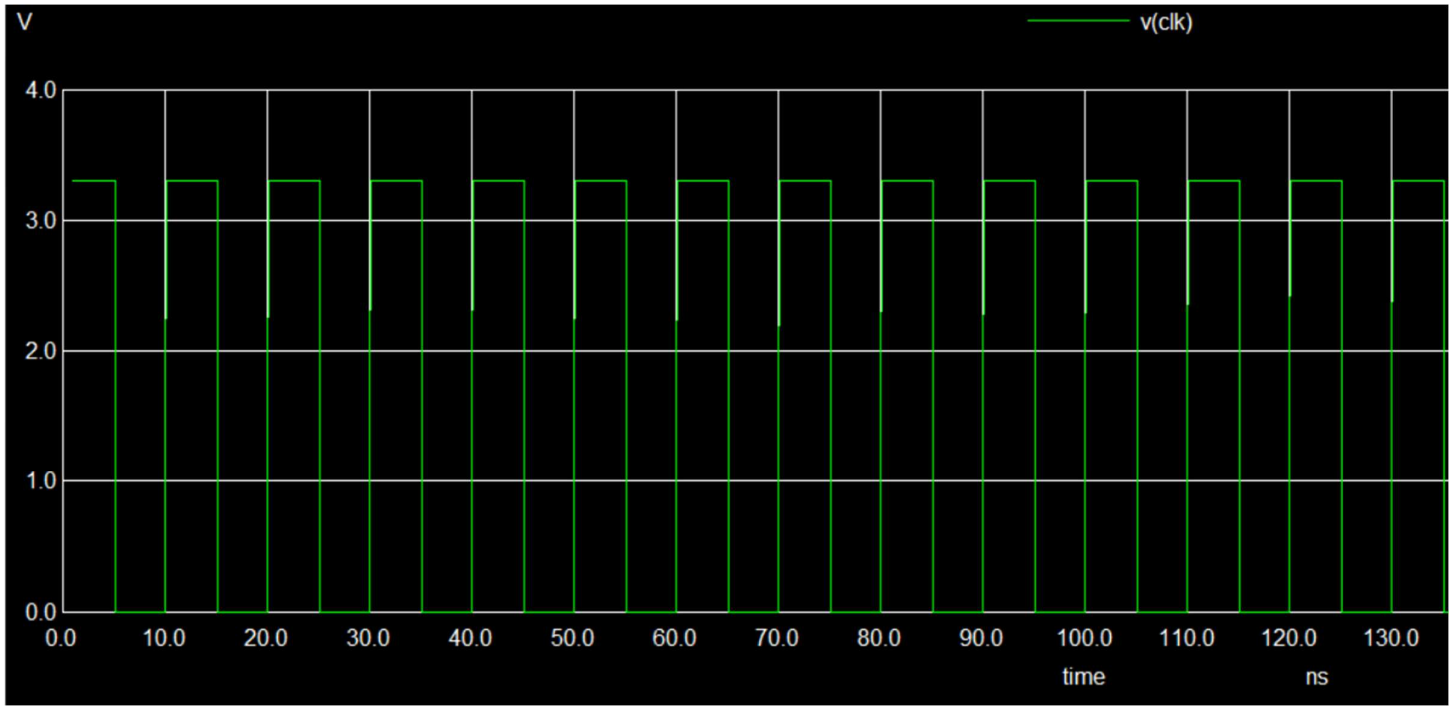
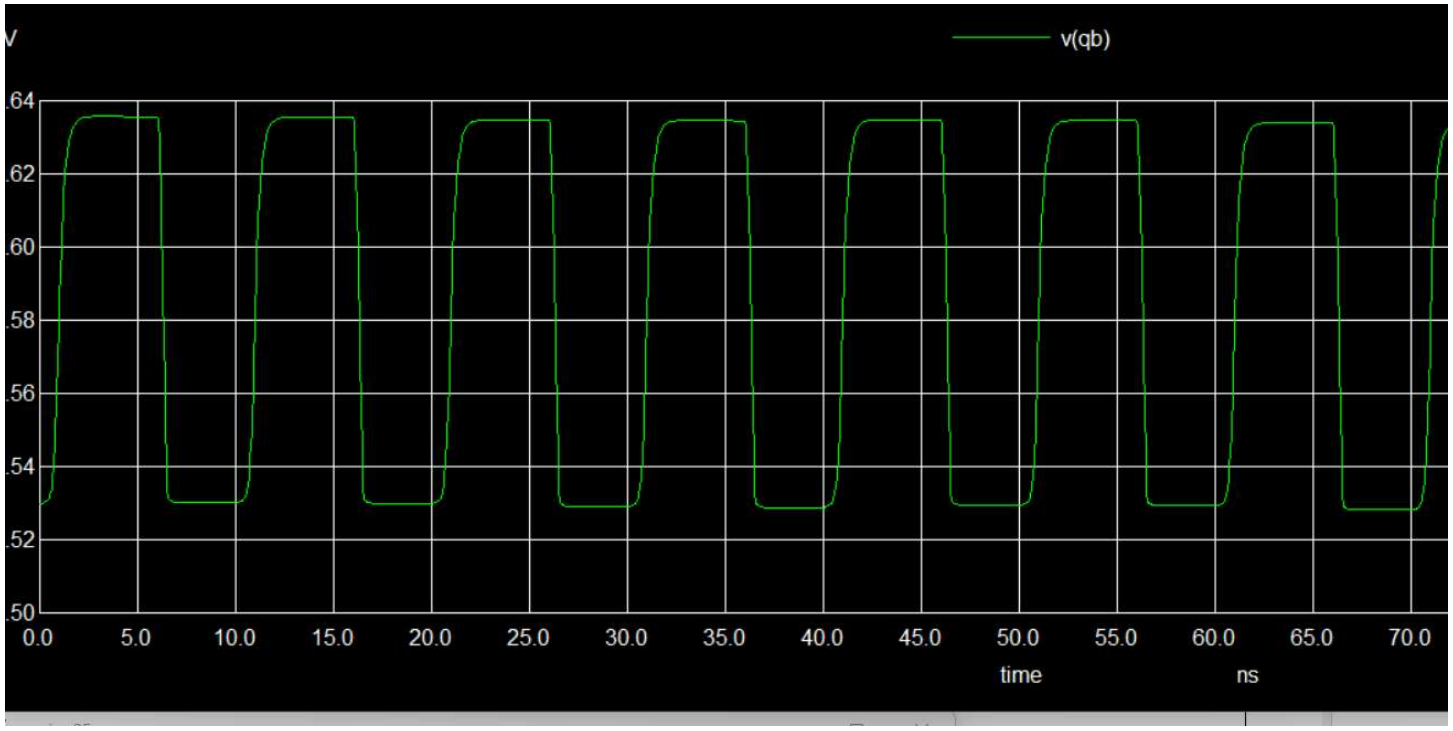


Fig: Input waveforms of BCD to Seven Segment

OUTPUT WAVEFORM:



CONCLUSION:

The Cross Charge Control Flip-Flop (XCFF) presents an effective solution for reducing power consumption in sequential circuits by minimizing internal switching activity and clock loading. By dividing the dynamic node into two independent nodes and enabling selective charge transfer based on input data, XCFF significantly lowers dynamic power dissipation while maintaining high-speed operation. The implicit pulse generation mechanism further enhances energy efficiency without increasing circuit complexity.

However, the XCFF architecture also exhibits limitations such as unwanted internal node precharging and increased hold time due to charge sharing effects. These challenges highlight the need for careful circuit optimization to improve robustness and timing reliability. Overall, XCFF demonstrates strong potential for low-power VLSI applications, provided its design constraints are appropriately addressed.

REFERENCE:

A. Hirata, K. Nakanishi, M. Nozoe, and A. Miyoshi, “The cross charge-control flip-flop: a low-power and high-speed flip-flop suitable for mobile application SoCs,” in Digest of Technical Papers. 2005 Symposium on VLSI Circuits, 2005., Kyoto, Japan, 2005, pp. 306–307. doi: 10.1109/VLSIC.2005.1469392.