

# Modeling and Simulation of SiC JFET using the Shichman–Hodges Model

Based on: “Modeling of Dynamic Properties of SiC JFETs”

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## 1. Theory / Description

Silicon Carbide (SiC) Junction Field-Effect Transistors (JFETs) are power semiconductor devices known for their high breakdown voltage, low ON-resistance, and fast switching characteristics. However, modeling their nonlinear current–voltage relationship and dynamic capacitances is essential for accurate simulation in circuit environments.

This work uses the Shichman–Hodges analytical framework to describe the drain current as:

$$I_D = \beta(V_{GS} - V_{TO})^2(1 + \lambda V_{DS})$$

where:

- $\beta$  – transconductance parameter (A/V<sup>2</sup>)
- $V_{TO}$  – threshold voltage
- $\lambda$  – channel-length modulation coefficient

In the eSim (Ngspice) implementation, the channel is represented using a voltage-controlled current source, while the gate–source and gate–drain junctions are modeled with diodes and parasitic capacitances ( $C_{gs}$ ,  $C_{gd}$ ). This provides an accurate representation of both steady-state and transient JFET behavior.

## 2. Circuit Diagram

## 3. Results / Outputs

The transient simulation was performed using Ngspice with:

- Supply voltage:  $V_{DD} = 12$  V
- Gate pulse: `PULSE(0 5 0 1u 1u 1m 2m)`

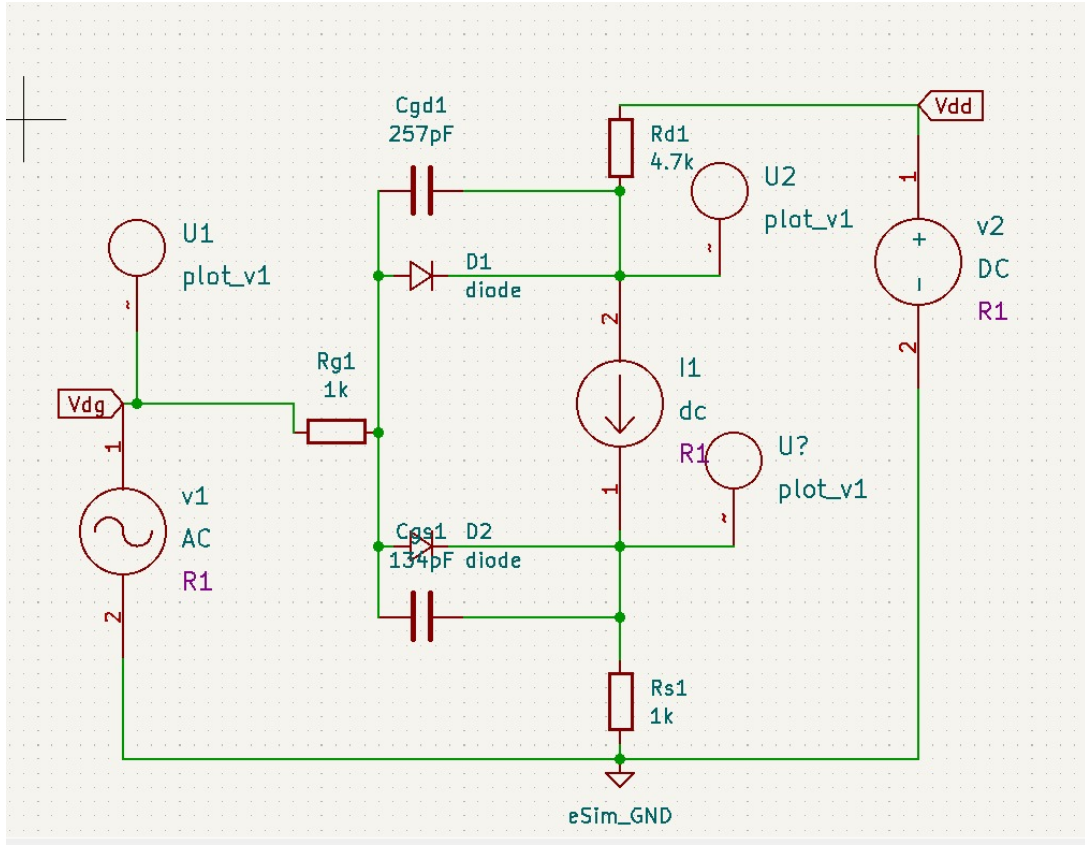


Figure 1: JFET Shichman–Hodges model schematic used for simulation in eSim/Ngspice.

- Drain resistor:  $R_D = 4.7 \text{ k}\Omega$

The gate voltage alternates between 0 V and 5 V, switching the JFET between ON and OFF states. The drain voltage waveform confirms proper switching action.



Figure 2: Ngspice transient simulation output showing gate and drain voltage waveforms.

Optional post-processing and waveform verification can also be done using Python (Matplotlib) to plot exported CSV simulation data.

## 4. References

1. Anna Bargieł, Przemysław Szulim, Jarosław Mroczka, “Modeling of Dynamic Properties of SiC JFETs,” *Electronics*, MDPI, Vol. 12, Issue 3, Article 459, pp. 1–14, 2023.
2. Ngspice / eSim Documentation – IIT Bombay, Open Source EDA Tool.
3. Shichman, H., and Hodges, D., “Modeling and Simulation of MOS Transistors,” *IEEE J. Solid-State Circuits*, 1968.