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Title of the circuit: Design and Simulation of 1-Bit ALU (Arithmetic and Logic Unit)

Theory/Description:

An **Arithmetic Logic Unit (ALU)** is the core computational block of a digital processor. It performs arithmetic and logical operations on input data and provides the result along with auxiliary signals such as carry or overflow. The 1-bit ALU designed here operates on two single-bit inputs and demonstrates the basic principles used in constructing larger multi-bit ALUs.

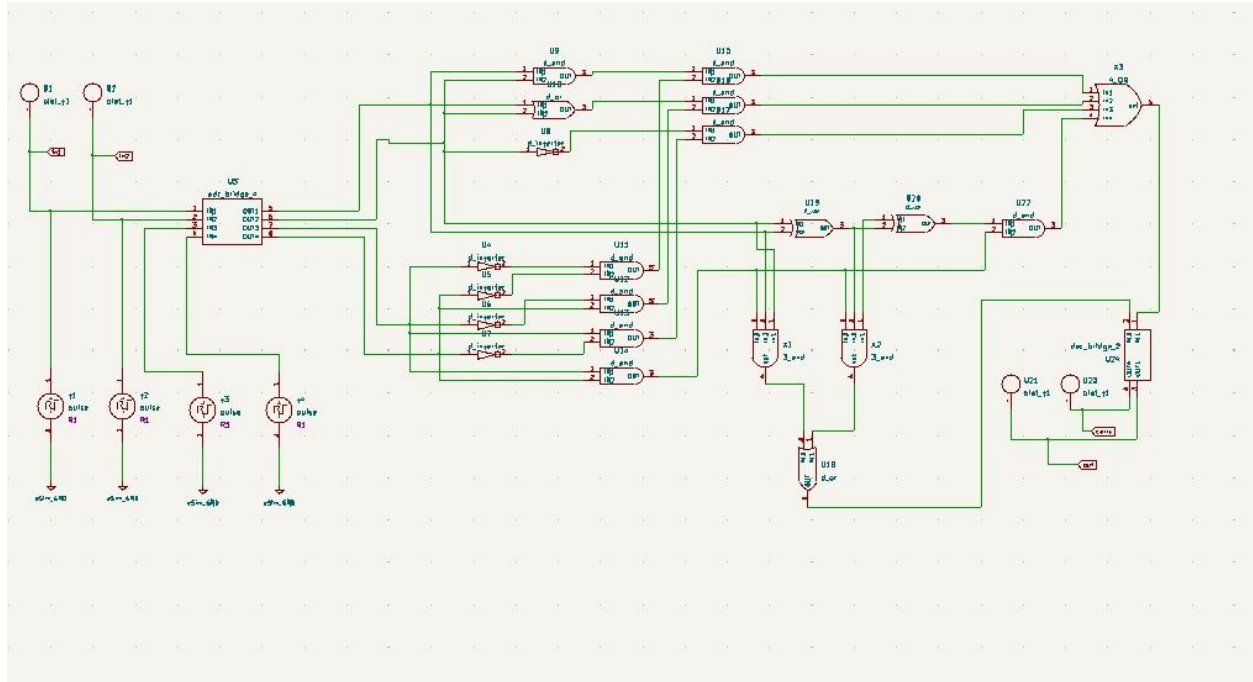
The circuit accepts two data inputs (IN1 and IN2) and a set of control signals that select the desired function. Logical operations such as AND, OR, and XOR are implemented using basic logic gates, while arithmetic operations such as addition and subtraction are performed using a full adder circuit. A multiplexer (MUX) is used to select the final output from the various logic and arithmetic results based on the control inputs.

In this design, the 1-bit ALU produces a single-bit output (OUT) and a carry output (CARRY) for arithmetic operations. By cascading multiple 1-bit units, multi-bit ALUs can be realized to handle larger word lengths.

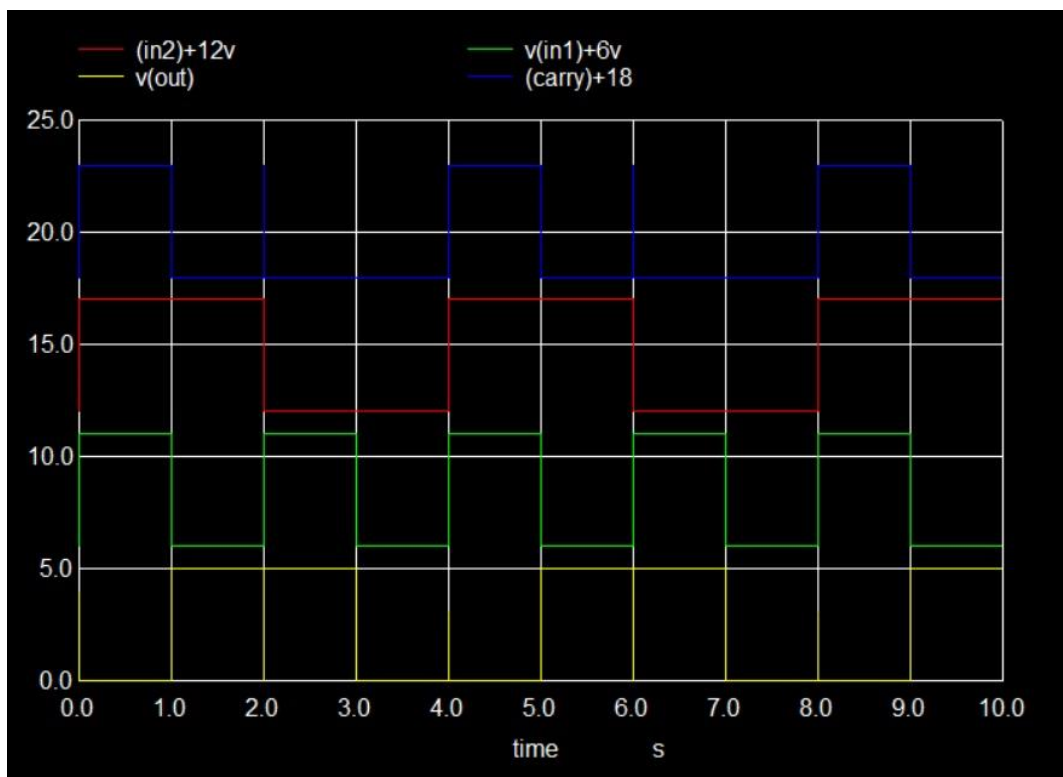
The schematic was designed and simulated using a digital design environment. The simulation waveform confirms the correct functionality of the circuit:

- The input signals **IN1** and **IN2** vary over time.
- The **OUT** waveform changes according to the selected operation.
- The **CARRY** output appears during arithmetic operations, verifying proper addition logic.

Circuit Diagram(s):



Results (Input, Output waveforms and/or Multimeter readings):



Source/Reference(s):

1. Raj Lakshmi Shukla and Rajesh Mehra, "Design Analysis and Simulation of 1-bit Arithmetic Logic Unit on Different Foundaries," Proceedings of National Conference on Recent Advances in Electronics and Communication Engineering (RACE-2014), NITTTR Chandigarh, March 28-29, 2014