

TSPC D FLIP FLOP

ABSTRACT

The True Single-Phase Clock (TSPC) D flip-flop offers high-speed and low-power operation by utilizing a single clock phase across all stages. The proposed design is negative-edge triggered, employing non-precharged N, precharged P, and non-precharged P stages, with an additional inverter to generate the complementary output. The circuit consists of 12 transistors including reset logic, and simulations confirm correct flip-flop functionality. While TSPC achieves low power and fast switching, its dynamic nature limits operation to MHz frequencies due to leakage effects at low clock rates.

INTRODUCTION

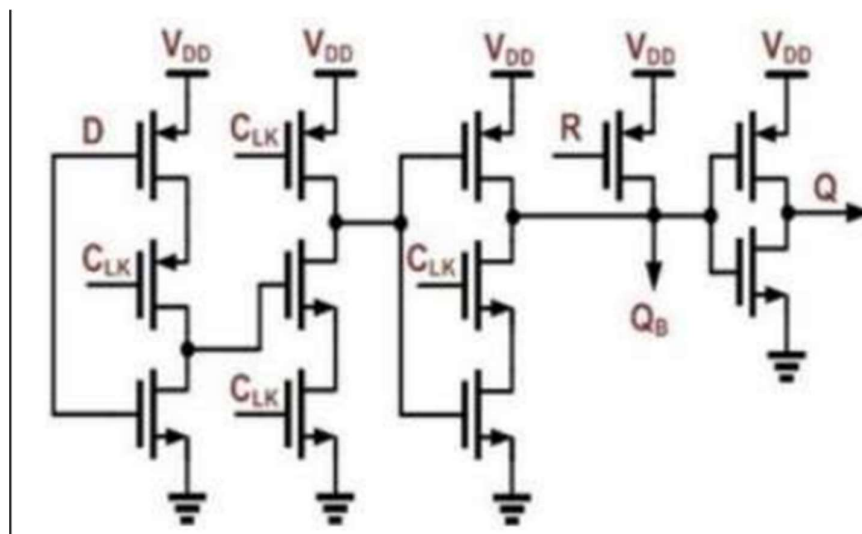
Flip-flops are fundamental sequential elements in digital systems, used to store and transfer data synchronized with a clock signal. Among various architectures, the True Single-Phase Clock (TSPC) D flip-flop has gained prominence due to its low power consumption, reduced transistor count, and high operating speed. Unlike conventional flip-flops that require complementary clock phases, TSPC uses only a single-phase clock, simplifying the clock distribution network and improving efficiency.

In a TSPC flip-flop, the design relies on dynamic logic principles, where parasitic capacitances temporarily store charge during operation. A typical implementation uses negative-edge triggering, since NMOS devices provide stronger pull-down characteristics, enhancing performance in CMOS technology. The flip-flop is built using a sequence of non-precharged N, precharged P, and non-precharged P stages, followed by an inverter to generate complementary outputs.

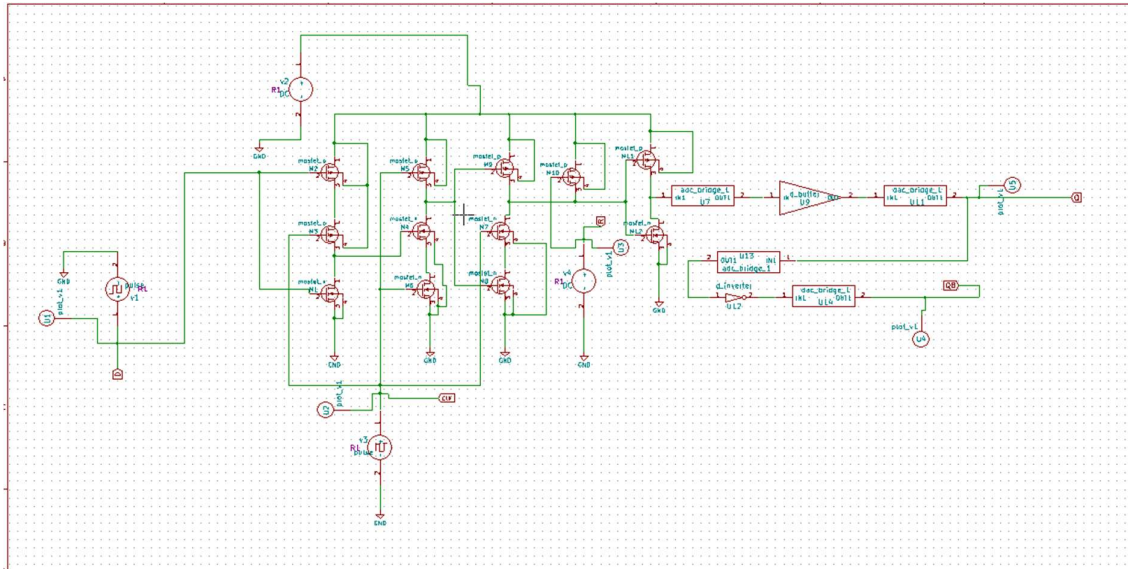
TSPC flip-flops are widely applied in high-speed and low-power digital circuits such as microprocessors, digital signal processors, and

communication systems. However, due to their dynamic nature, they are prone to leakage and can lose stored data at very low frequencies, making them suitable mainly for operation in the MHz to GHz range.

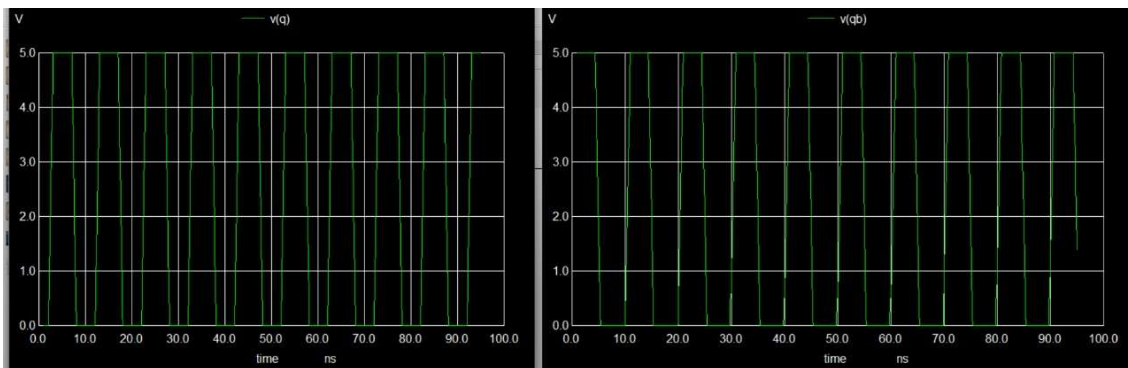
BLOCK DIAGRAM



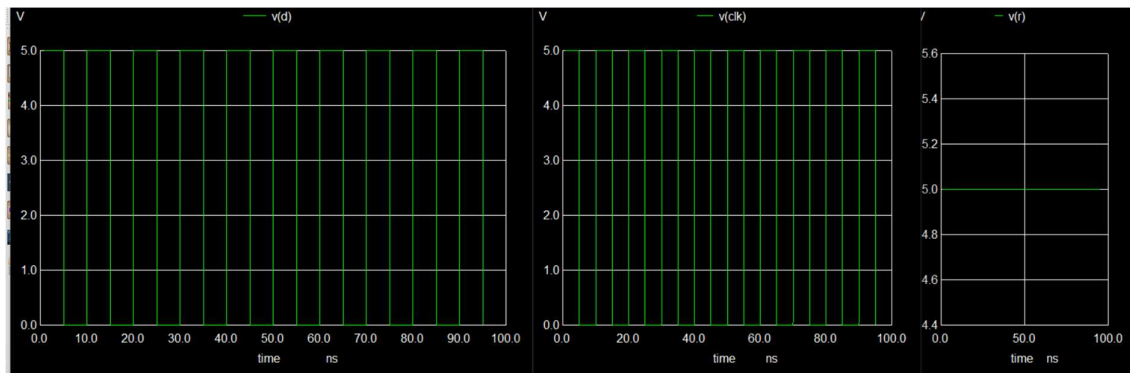
SCHEMATIC DIAGRAM



OUTPUT WAVEFORMS



INPUT WAVEFORMS



References:

[1] <https://ieeexplore.ieee.org/document/10150117>

Project submitted by:

Pandiyarajan S

Chennai institute of technology,