

# 4-Bit Baugh-Wooley Multiplier

Jovin P John  
Electronics and Communication  
Engineering  
Albertian Institute of Science and  
Technology  
Kochi, Kerala

**Abstract—** This project implements a 4-bit Baugh-Wooley multiplier for multiplying two signed binary numbers in two's complement format. The design uses modified partial product generation with systematic array of adders. The circuit directly handles signed multiplication without requiring separate sign processing logic.

**Keywords—** Baugh-Wooley Multiplier, Signed Multiplication, Two's Complement, Array Multiplier

## I. INTRODUCTION

A 4-bit Baugh-Wooley multiplier is a digital circuit designed to multiply two 4-bit signed numbers represented in two's complement format. Unlike unsigned multipliers, this design incorporates special modifications to handle sign bits directly, eliminating the need for additional sign correction circuitry.

## II. OBJECTIVES

The aim of this project is to design a 4-bit Baugh-Wooley multiplier that correctly multiplies two signed BCD

numbers producing an 8-bit result. The project focuses on implementing modified partial product generation and systematic adder arrangement. The goal is to build the truth table, run transient analysis simulation, and confirm that the multiplier works for all signed input combinations.

## III. IMPLEMENTATION

The Baugh-Wooley multiplier uses modified partial product generators arranged in a systematic array with full adders and half adders. Special logic handles sign bit interactions through inversions and corrections. The array structure processes partial products systematically to generate the final 8-bit signed product ( $S_7-S_0$ ).

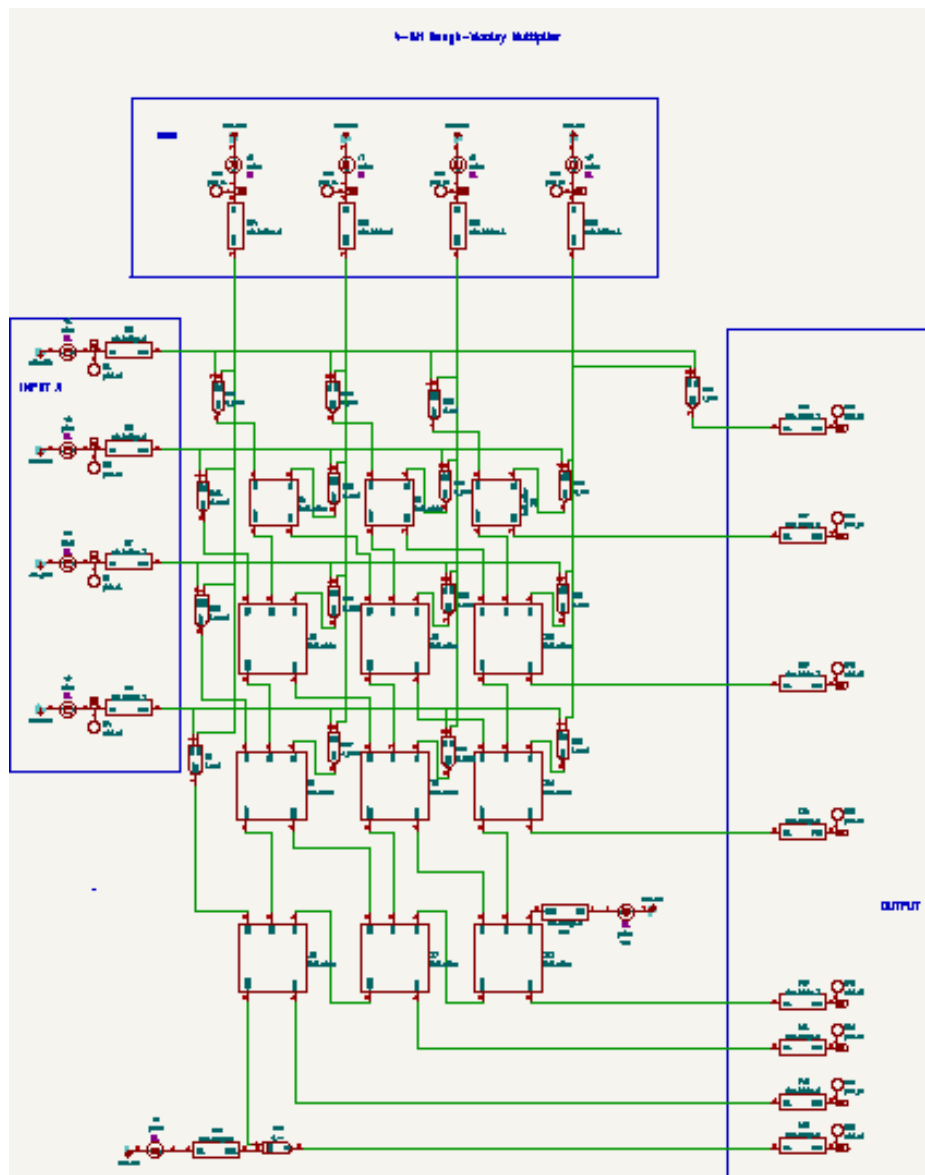


Fig. 1. eSim Circuit Schematic

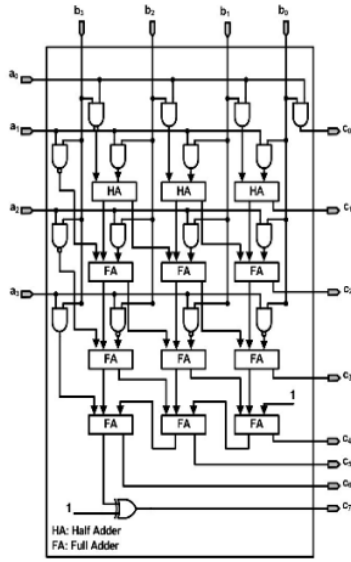


Fig. 2. Logic Diagram

#### IV. RESULTS

The 4-bit Baugh-Wooley Multiplier was implemented and tested in simulation. The truth table was prepared with inputs A and B ranging from 1111 to 0000, and the outputs  $S_7$ - $S_0$  were verified through transient analysis. The results confirm that the multiplier performs correct signed multiplication for all cases. Transient analysis showed proper handling of both positive and negative number combinations.

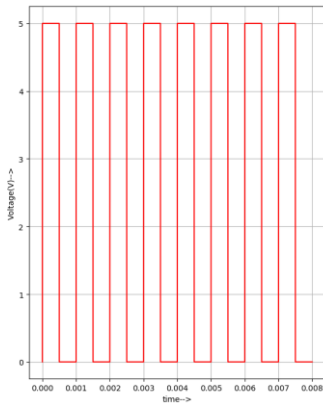


Fig. 3. Input A0

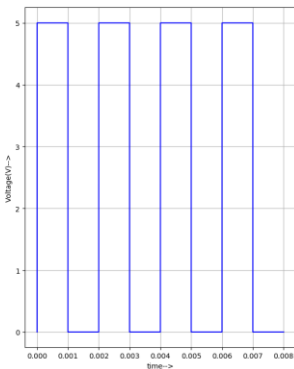


Fig. 4. Input A1

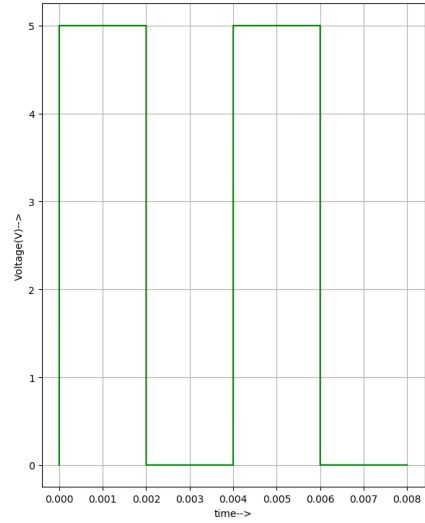


Fig. 5. Input A2

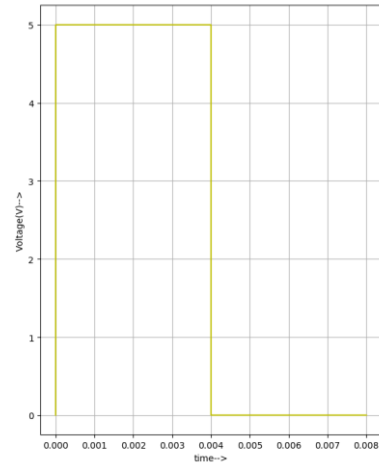


Fig. 6. Input A4

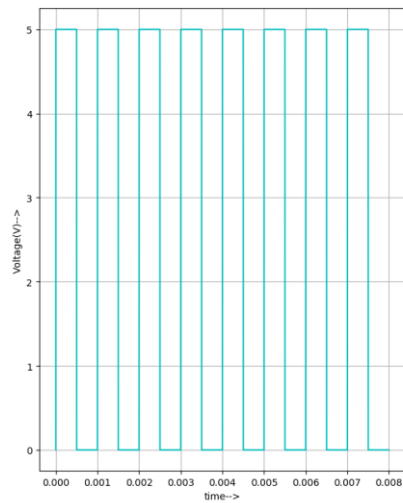


Fig. 7. Input B0

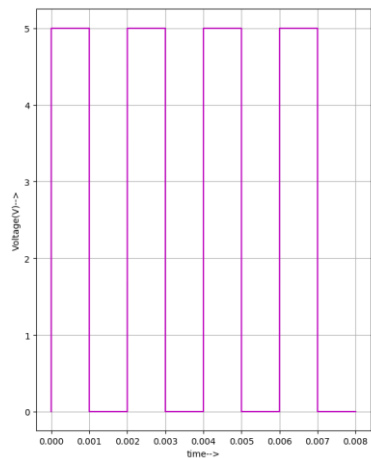


Fig. 8. Input B1

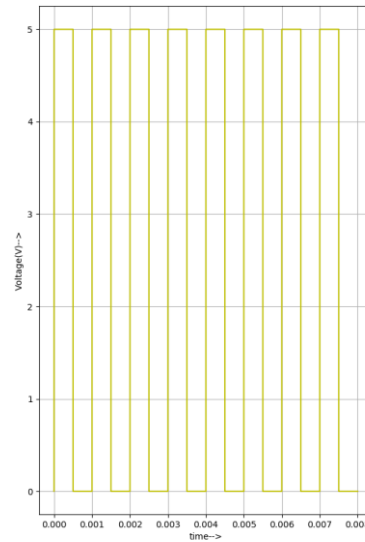


Fig. 11. Output O0

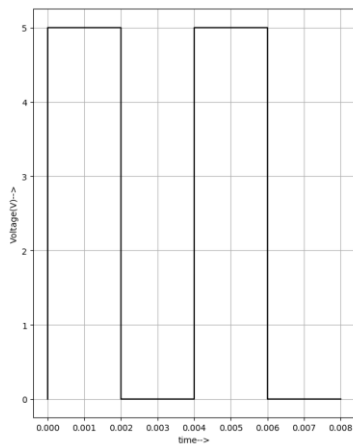


Fig. 9. Input B2

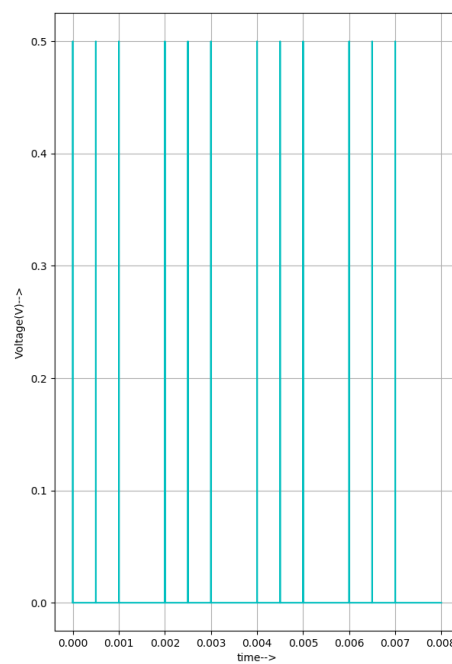


Fig. 12. Output O1

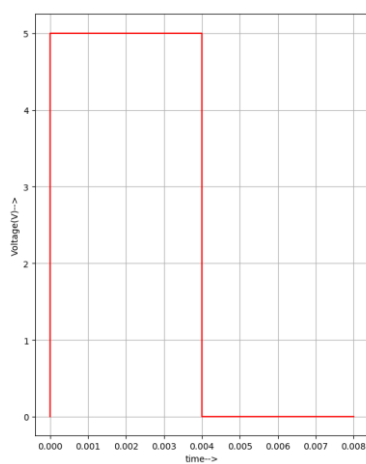


Fig. 10. Input B3

Figures 3 to 10 represent the four input bits of A and B.

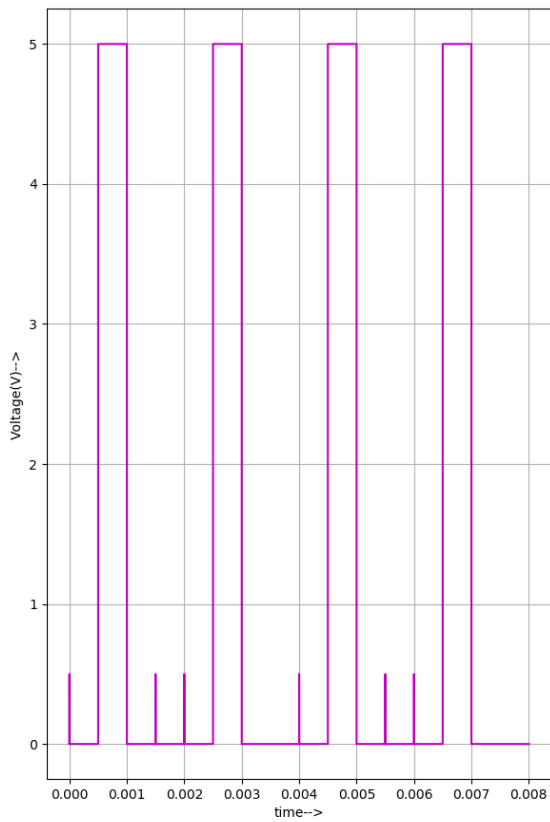


Fig. 13. Output O2

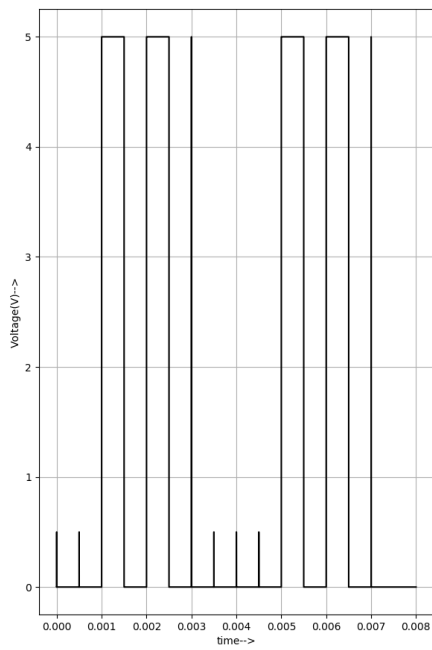


Fig. 14. Output O3

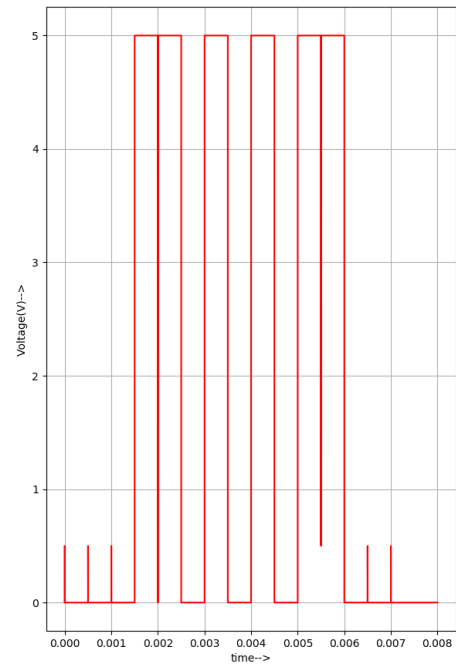


Fig. 15. Output O4

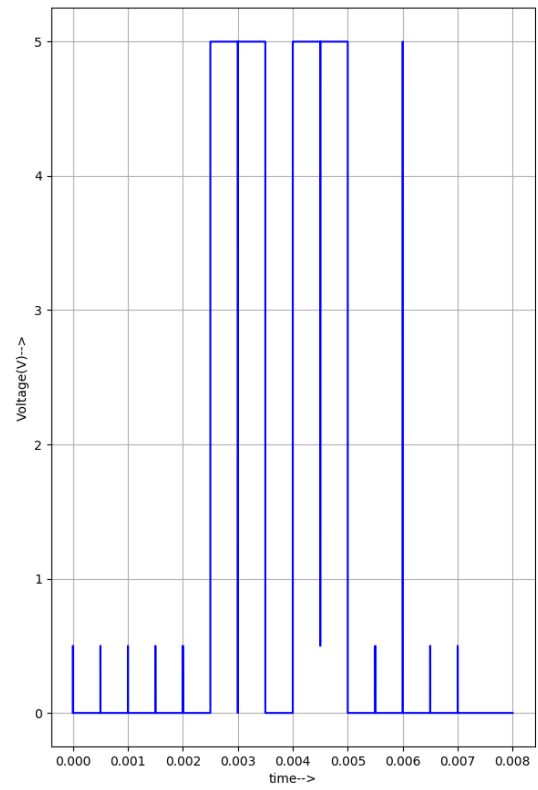


Fig. 16. Output O5

Figures 11 to 18 represents the output.

## V. ANALYSIS

The working of the 4-bit Baugh-Wooley Multiplier was verified using transient analysis. This analysis observed how the outputs ( $S_7-S_0$ ) changed over time when different input combinations for  $A_3-A_0$  and  $B_3-B_0$  were applied. The transient analysis waveforms confirmed correct timing, proper partial product generation, and accurate signed multiplication results. The timing analysis validated the array structure behavior during computation cycles.

## VI. CONCLUSION

The 4-bit Baugh-Wooley Multiplier was successfully implemented in eSim using modified partial product generators and systematic adder arrays. Transient analysis confirmed that the circuit produced correct signed multiplication outputs ( $S_7-S_0$ ) for different input combinations. The eSim simulation results showed proper timing behavior and accurate two's complement arithmetic. This design demonstrates an efficient method for signed multiplication in digital signal processing systems.

## REFERENCES

Kumar, N. V. N. P. (2017). Design and analysis of Booth multiplier using FPGA. *International Journal of Engineering Research and Application*

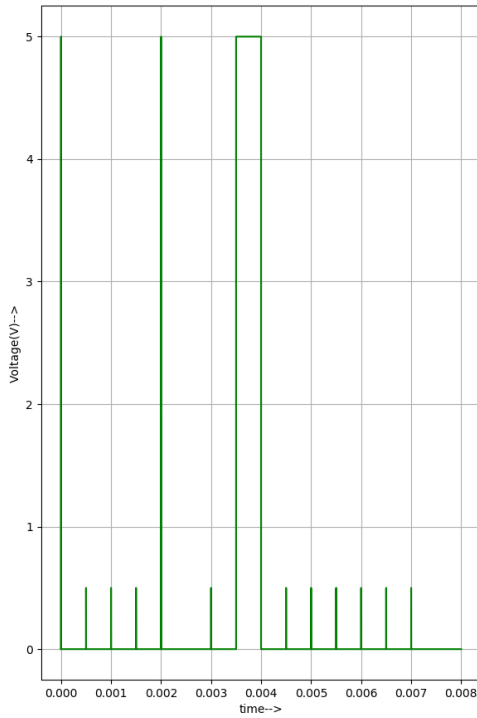


Fig. 17. Output 06

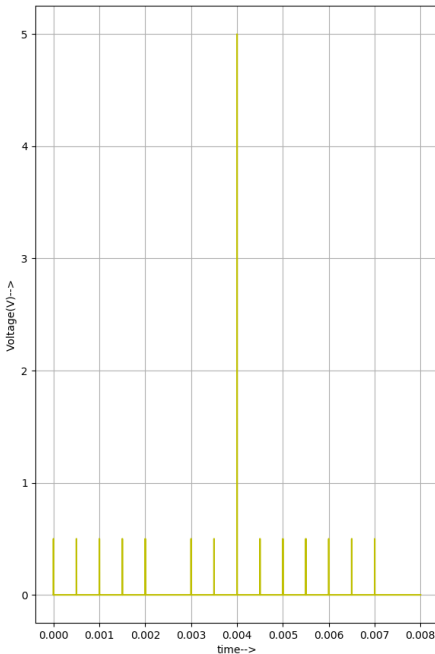


Fig. 18. Output 07