

Circuit Simulation Project

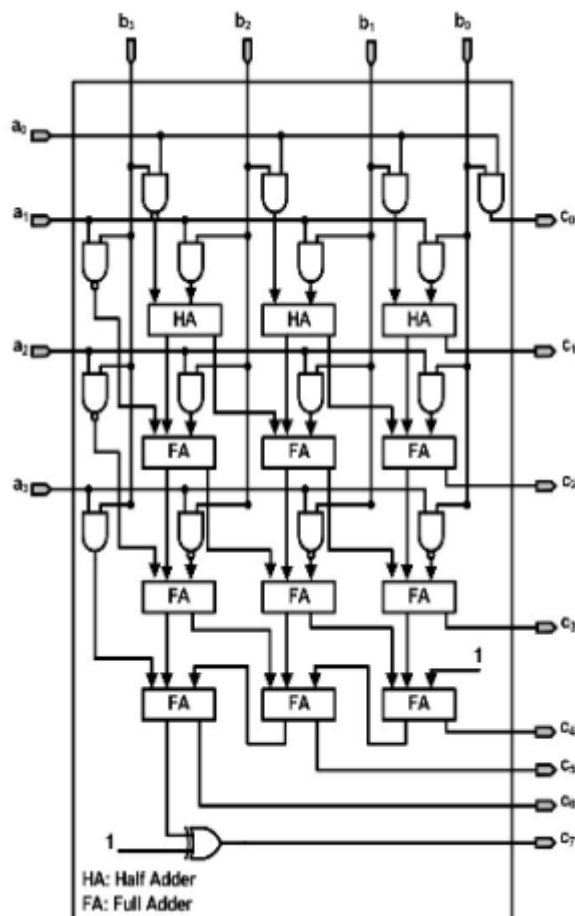
<https://esim.fossee.in/circuit-simulation-project>

Name of the participant : Jovin P John

Title of the circuit : 4-bit Baugh-Wooley Multiplier

Theory/Description : A 4-bit Baugh-Wooley multiplier is a circuit that directly multiplies two 4-bit signed numbers without separate sign handling. It uses a grid of logic gates and adders arranged systematically to generate the 8-bit product result. This design efficiently handles negative numbers using two's complement arithmetic in hardware.

Circuit Diagram(s) :



Results (Input, Output waveforms and/or Multimeter readings) :

A	B	S ₇	S ₆	S ₅	S ₄	S ₃	S ₂	S ₁	S ₀	Product (Decimal)
1111 (-1)	1111 (-1)	0	0	0	0	0	0	0	1	1
1110 (-2)	1110 (-2)	0	0	0	0	0	1	0	0	4
1101 (-3)	1101 (-3)	0	0	0	0	1	0	0	1	9
1100 (-4)	1100 (-4)	0	0	0	1	0	0	0	0	16
1011 (-5)	1011 (-5)	0	0	0	1	1	0	0	1	25
1010 (-6)	1010 (-6)	0	0	1	0	0	1	0	0	36
1001 (-7)	1001 (-7)	0	0	1	1	0	0	0	1	49
1000 (-8)	1000 (-8)	0	1	0	0	0	0	0	0	64
0111 (7)	0111 (7)	0	0	1	1	0	0	0	1	49
0110 (6)	0110 (6)	0	0	1	0	0	1	0	0	36
0101 (5)	0101 (5)	0	0	0	1	1	0	0	1	25
0100 (4)	0100 (4)	0	0	0	1	0	0	0	0	16
0011 (3)	0011 (3)	0	0	0	0	1	0	0	1	9
0010 (2)	0010 (2)	0	0	0	0	0	1	0	0	4
0001 (1)	0001 (1)	0	0	0	0	0	0	0	1	1
0000 (0)	0000 (0)	0	0	0	0	0	0	0	0	0

Source/Reference(s) : Kumar, N. V. N. P. (2017). Design and analysis of Booth multiplier using FPGA. International Journal of Engineering Research and Application