4-Bit 2’s Complement Adder/Subtractor

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***Abstract*— This project explains the design and working of a 4-bit 2’s Complement Adder/Subtractor. It performs both addition and subtraction of two 4-bit binary numbers using full adders and XOR logic. The control input selects between addition and subtraction by complementing one operand and adding a carry-in. Transient analysis was carried out to verify timing, correctness, and overflow detection.**

Keywords*— *2’s Complement, Adder, Subtractor, XOR Logic, Transient Analysis

I. Introduction

A 4-bit 2’s Complement Adder/Subtractor is a digital circuit that performs both addition and subtraction on binary numbers. The operation depends on a control signal: when the signal is low, the circuit performs addition; when high, it performs subtraction. This is achieved by XORing each bit of the second operand with the control signal and using the same signal as the initial carry-in. The circuit handles signed numbers and also detects overflow when results exceed the representable range.

II. Objectives

The aim of this project is to design a 4-bit 2’s Complement Adder/Subtractor that can perform both addition and subtraction using a single circuit. The focus is on showing how XOR logic modifies one operand to support subtraction. The objectives include constructing the truth table, testing overflow behavior, running transient analysis, and verifying correct outputs in all cases.

III. Implementation

The 4-bit 2’s Complement Adder/Subtractor is implemented using four full adders and XOR gates. Each bit of the second operand is XORed with the add/subtract control signal, and the control signal is also used as the carry-in to the least significant full adder. For addition, the operand is passed unchanged, while for subtraction, the operand is complemented and incremented by one (2’s complement). The full adders then produce the sum or difference bits along with the carry and overflow flags. The circuit was built and simulated in eSim for verification.

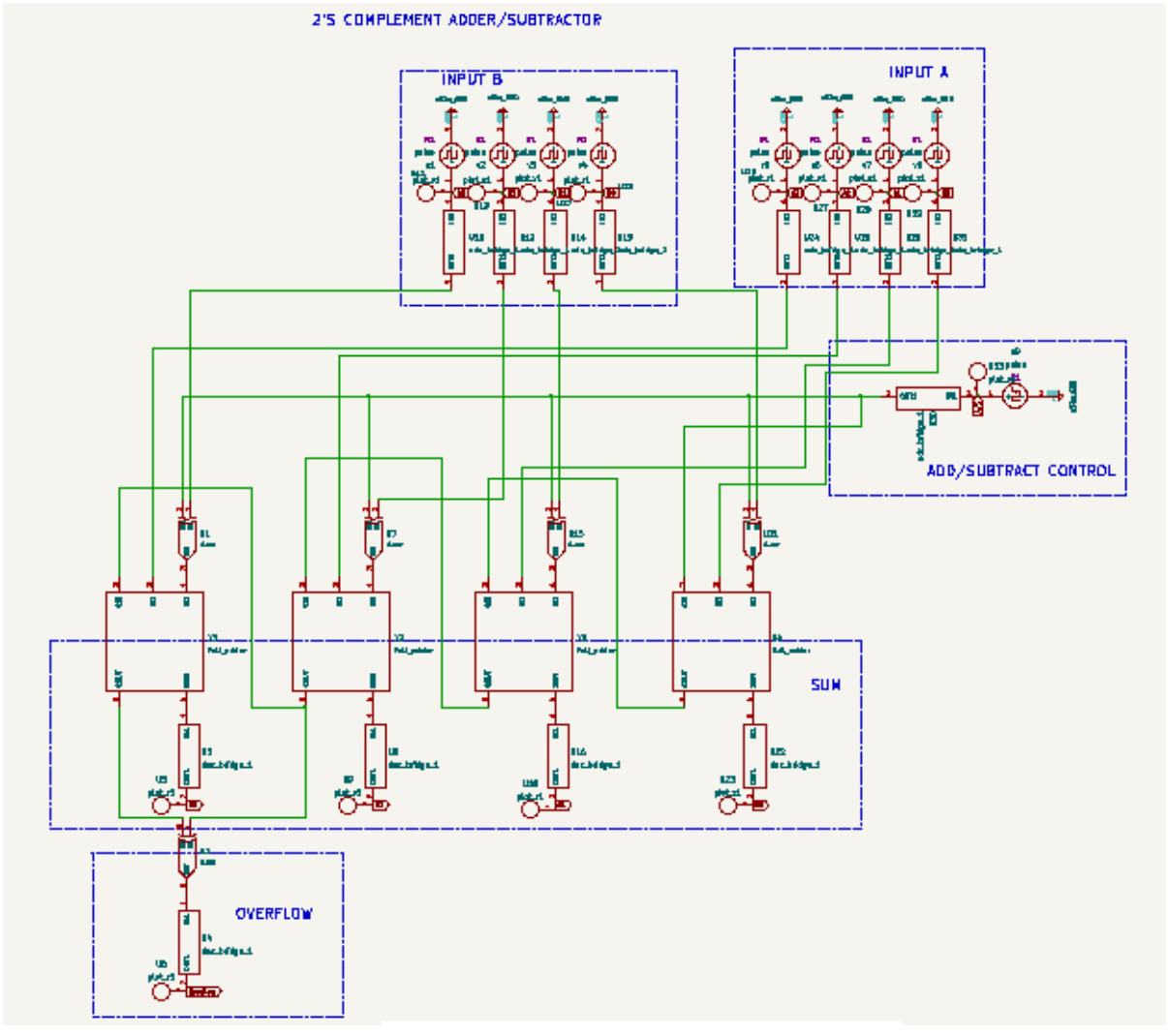

Fig. 1. eSim Circuit Schematic

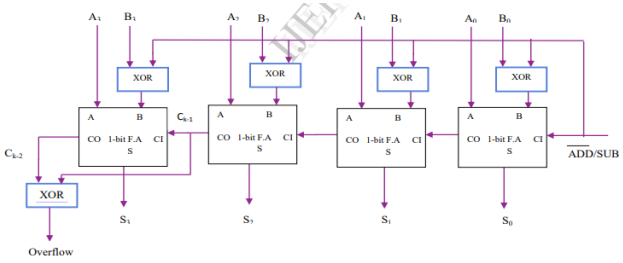

Fig. 2. Logic Diagram

IV. Results

The 4-bit 2's Complement Adder/Subtractor was implemented and tested. The truth table was prepared with inputs ranging from 1111 to 0000 for both operands, and the outputs of sum (S0–S3) and overflow (OVF) were verified. Transient analysis was performed to observe timing behavior. The results confirmed correct binary addition when the control signal was low and correct subtraction when the control signal was high.

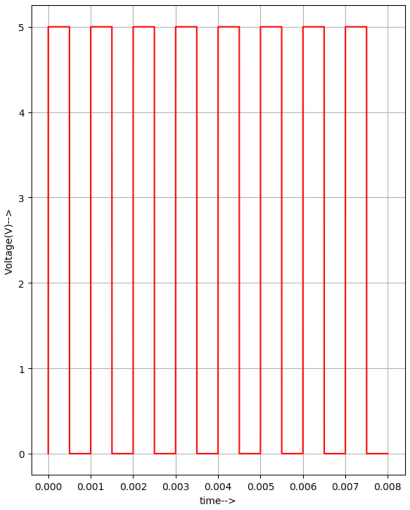

Fig. 3. Input A0

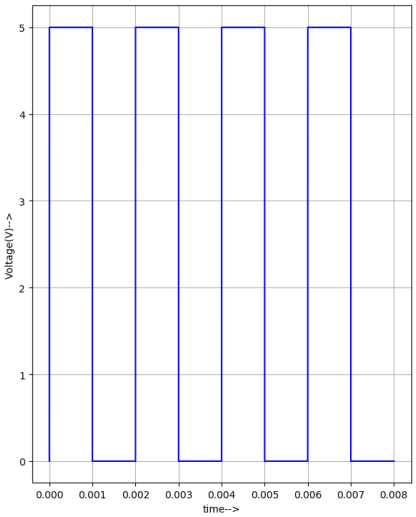

Fig. 4. Input A1

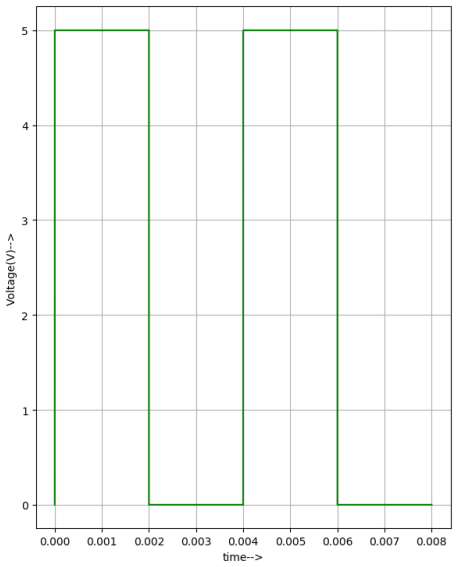

Fig. 5. Input A2

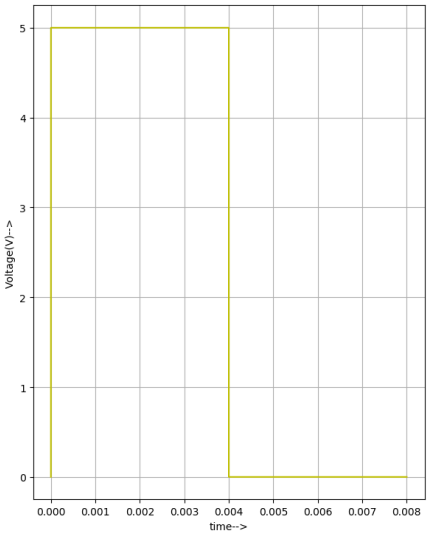

Fig. 6. Input A4

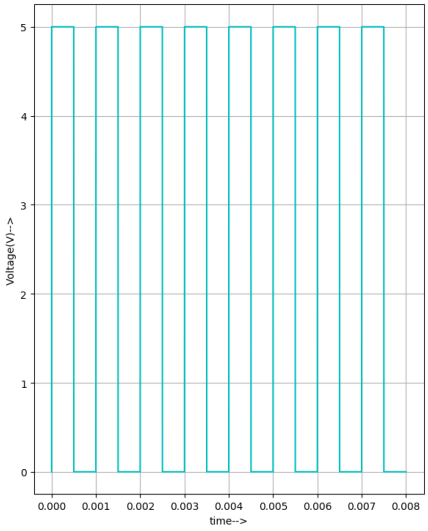

Fig. 7. Input B0

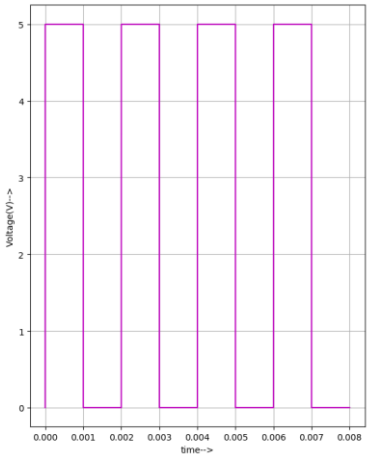

Fig. 8. Input B1

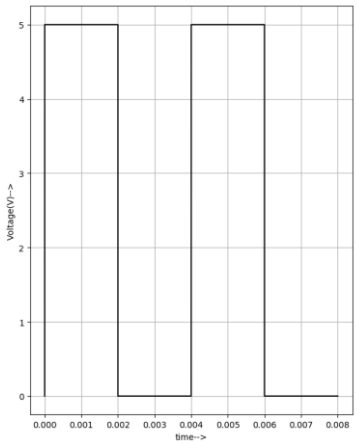

Fig. 9. Input B2

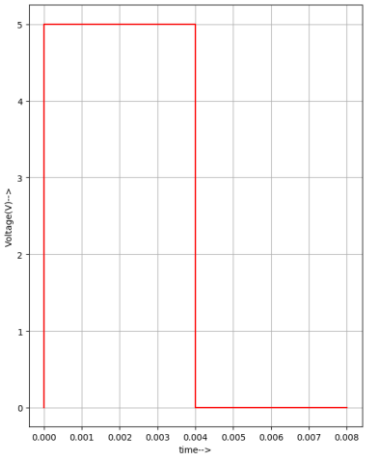

Fig. 10. Input B3

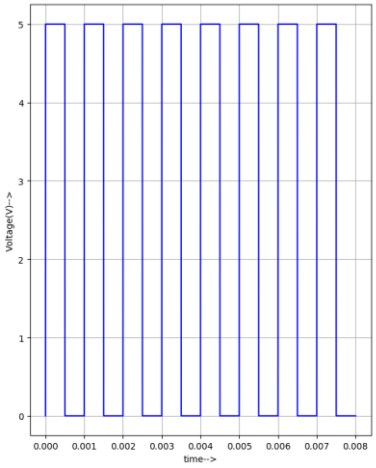

Fig. 11. Input A/S Control

Figures 3 to 11 represent the four input bits of A and A/S control.

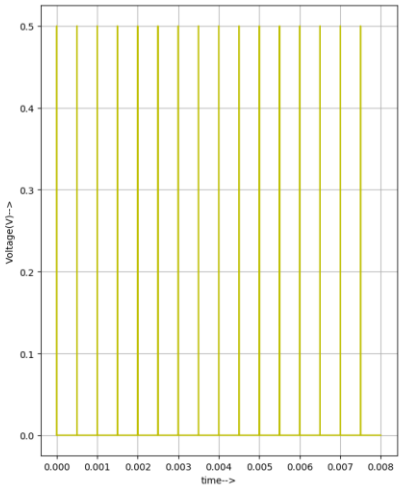

Fig. 12. Output S0

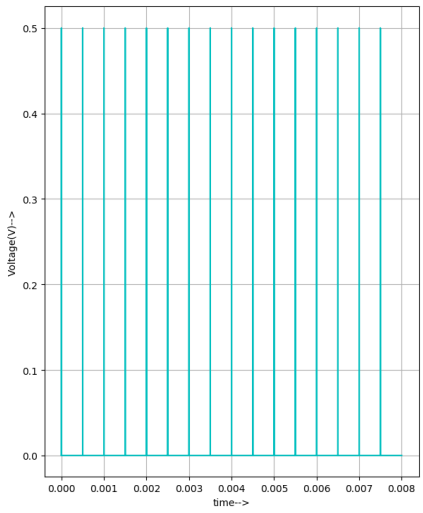

Fig. 13. Output S1

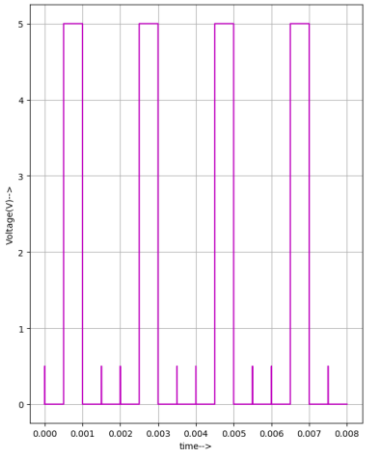

Fig. 14. Output S2

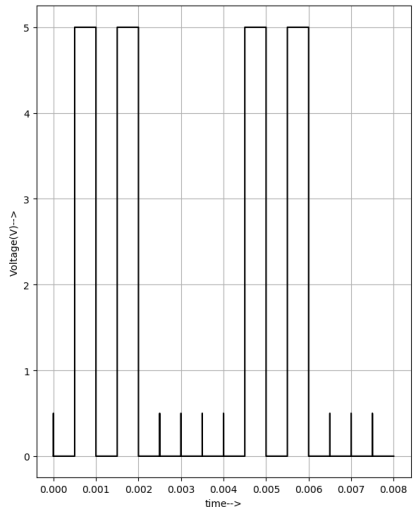

Fig. 15. Output S3

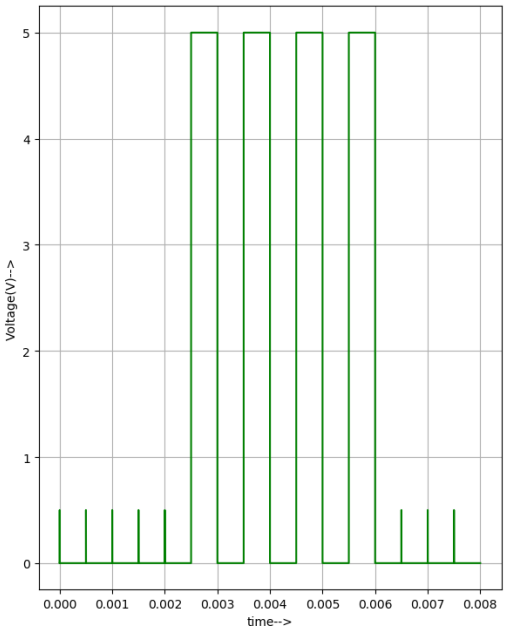

Fig. 16. Overflow

Figures 12 to 16 represents the sum bits and overflow.

V. Analysis

The working of the 2's Complement Adder/Subtractor was verified using transient analysis. The waveforms displayed the switching of sum outputs and the overflow signal. The results confirmed that the circuit correctly performed addition and subtraction, handled signed numbers, and detected overflow when results exceeded the 4-bit range. The XOR logic was observed to properly modify the operand for subtraction, ensuring accurate operation.

VI. Conclusion

The 4-bit 2's Complement Adder/Subtractor was successfully implemented in eSim using full adders and XOR gates. Transient analysis confirmed that the circuit produced correct results for both addition and subtraction. The circuit correctly generated the overflow signal and maintained proper timing. The design demonstrated an efficient way of combining both operations in a single hardware structure.

References

Ajitha, D., Kumar, P. Y., Ramanaiah, K. V., & Sumalatha, V. (2013). Efficient design of 2's complement adder/subtractor using QCA. *International Journal of Engineering Research & Technology (IJERT)*