

# A Low-Power and High-Speed Dynamic PLA Circuit Configuration for Single-Clock CMOS

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## Abstract

Programmable Logic Arrays (PLAs) are fundamental building blocks in VLSI processors and control units, providing flexible implementation of complex Boolean functions that are difficult to realize using random logic. Traditional PLA designs face significant challenges including racing problems, high power dissipation, charge sharing issues, and the need for multiple clock phases. The demand for low-power, high-speed digital circuits has made efficient PLA design a critical area of research in modern CMOS technology.

This paper presents the design and performance analysis of a novel low-power, high-speed dynamic PLA circuit configuration using single-phase clock operation. The proposed architecture employs a strategic combination of dynamic logic, buffering techniques, and optimized transistor arrangements to overcome the limitations of conventional PLA designs. The key innovation involves inserting buffering static NAND gates between NOR planes to eliminate racing problems and reduce glitch duration, thereby significantly reducing dynamic power consumption while maintaining high-speed operation.

The proposed PLA has been implemented using 0.6 $\mu$ m CMOS technology and evaluated against various existing architectures including pseudo-NMOS, NOR-NOR, domino logic, and other state-of-the-art designs. Performance analysis demonstrates superior characteristics in terms of propagation delay, power consumption, and power-delay product. The circuit achieves zero static power dissipation, eliminates ground switches, prevents charge sharing, and operates with full voltage swing output.

## I. INTRODUCTION

Programmable Logic Arrays (PLAs) are essential building blocks in VLSI design, particularly valuable for implementing control units and complex Boolean functions that are challenging to realize through conventional random logic approaches. As integrated circuit technology continues to advance toward higher device densities and lower supply voltages, the demand for efficient PLA implementations has become increasingly critical. PLAs offer the flexibility to implement virtually any Boolean function, making them indispensable in both combinational and sequential circuit design.

Traditional PLA architectures face several significant challenges that limit their performance in modern applications. Pseudo-NMOS designs suffer from DC path dissipation and ratioed design constraints that reduce speed and increase power consumption. Dynamic NOR-NOR implementations encounter racing problems when cascading dynamic gates, necessitating delayed clocks that compromise operational speed. Domino logic approaches, while offering excellent power characteristics, introduce serial NMOS transistor delays and potential charge-sharing issues that degrade performance.

This research focuses on developing a revolutionary single-clock dynamic PLA architecture that addresses these fundamental limitations. The proposed design strategically combines dynamic logic principles with intelligent buffering techniques to achieve optimal performance characteristics. By inserting buffering NAND gates between NOR planes, the architecture eliminates racing problems, reduces power consumption, and enhances operational speed while maintaining design simplicity.

The significance of this work extends beyond individual PLA performance, contributing to broader advancements in low-power VLSI design methodologies. As modern processors demand increasingly efficient control logic implementations, the proposed PLA design offers a robust solution that meets contemporary performance requirements while supporting future scaling trends in semiconductor technology.

## II. PURPOSE OF DYNAMIC PLA CIRCUIT:

The purpose of this low-power high-speed dynamic PLA circuit configuration is:

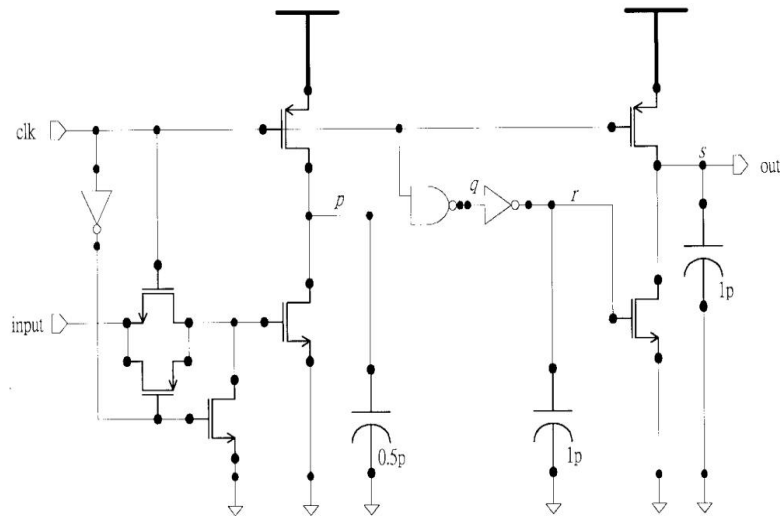
- **Boolean Function Implementation** – It efficiently implements complex Boolean functions that are difficult to realize using conventional random logic, particularly for control units in VLSI processors and digital systems.
- **Single-Clock Operation** – Eliminates the need for multiple clock phases and delayed clocks, simplifying timing design and reducing clock skew issues while enhancing overall system reliability.
- **Power Optimization** – Achieves zero static power dissipation through dynamic operation while significantly reducing dynamic power consumption by minimizing switching activity and glitch duration.
- **Racing Problem Elimination** – The buffering NAND gate architecture prevents racing conditions between cascaded dynamic logic stages, ensuring correct logic operation without requiring delayed clock signals.
- **High-Speed Performance** – Delivers superior propagation delay characteristics by eliminating ground switches, reducing parasitic capacitances, and optimizing charge/discharge paths for enhanced switching speed.

### III. WORKING PRINCIPLE:

The working principle of the low-power high-speed dynamic PLA circuit is based on the strategic integration of dynamic logic techniques with intelligent buffering to achieve optimal performance. Here are the key operational steps:

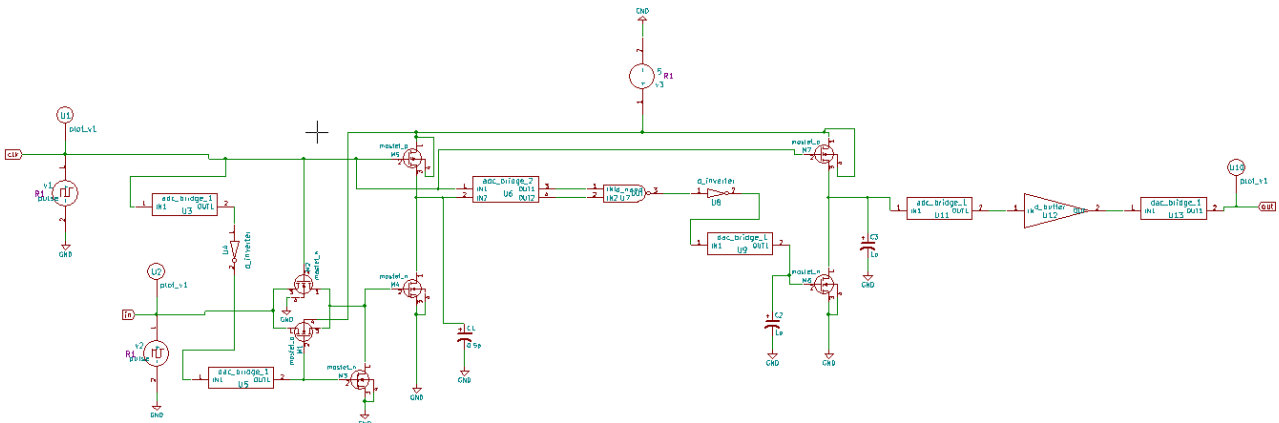
1. Clock Pre charge Phase (CLK = 0): During the pre charge phase, all inputs to the first NOR plane are disabled through the triggered one-bit decoder. Node p is charged to VDD, while the buffering NAND gate pre charges node q to high and pre discharges node r to ground, establishing proper initial conditions.
2. Input Signal Conditioning: The triggered one-bit decoder ANDs all input signals with the clock, ensuring that inputs are only active during the evaluation phase. This eliminates unwanted signal transitions during pre charge and reduces power consumption.
3. Evaluation Phase Activation (CLK = 1): When the clock transitions high, input signals are fed through the triggered decoder to the NMOS evaluation network. The buffering NAND gate simultaneously transforms into an inverter configuration, enabling signal propagation.
4. Logic Evaluation Process: If the pull-down NMOS network in the first stage evaluates to logic high, node p discharges to ground, maintaining nodes q and r in their respective high and low states. The output s remains unchanged from its previous state.
5. Output State Transition: If the pull-down network evaluates to logic low, node p remains high, causing the buffering NAND gate to flip states of q and r to low and high respectively. This results in the output s being discharged to ground through the second stage.
6. Power and Speed Optimization: The buffering NAND gate statistically reduces switching probability while eliminating the need for ground switches and delayed clocks, resulting in both reduced power consumption and enhanced operational speed.

### CIRCUIT DIAGRAM

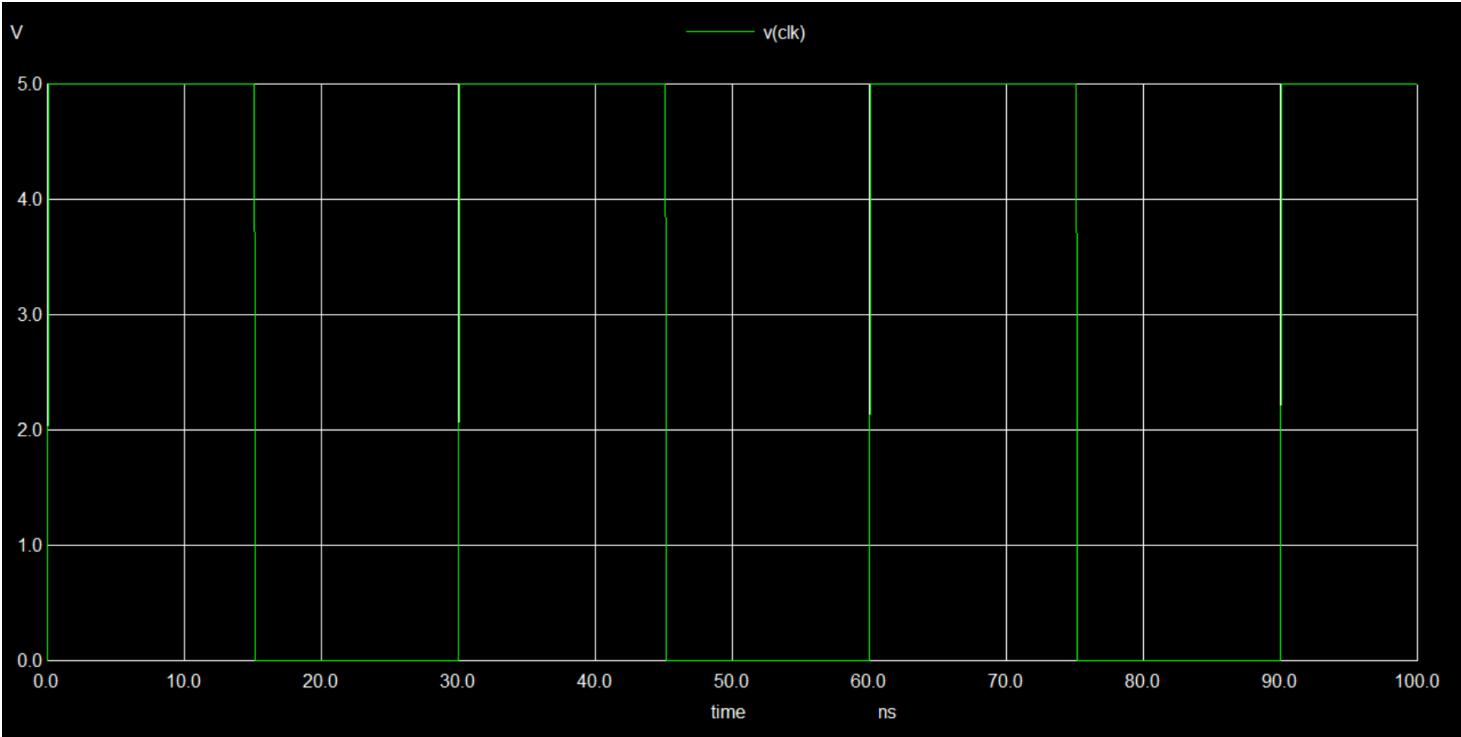
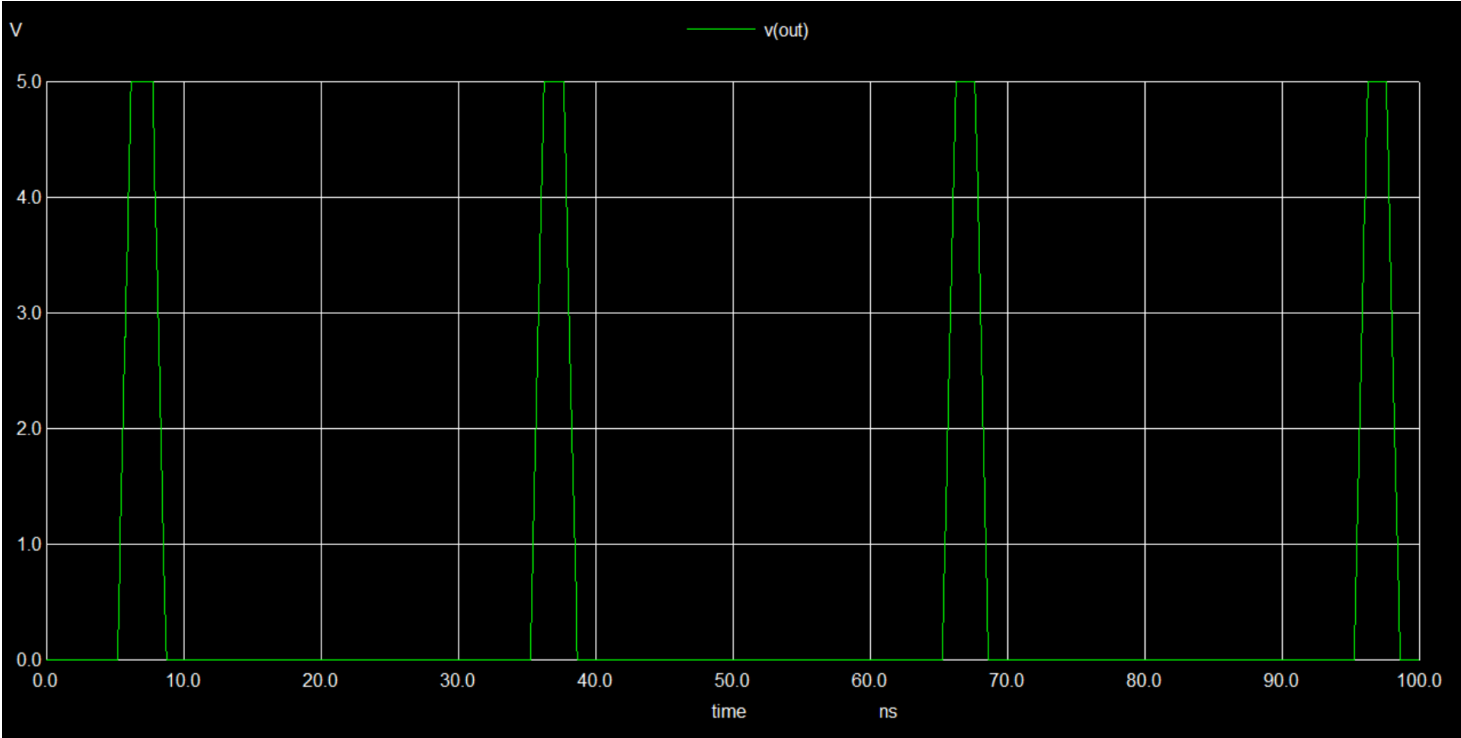


Low-power and high-speed PLA circuit.

### E-SIM IMPLEMENTATION :



OUTPUT WAVEFORMS :



## **CIRCUIT EXPLANATION:**

The low-power high-speed dynamic PLA circuit employs a strategic combination of triggered one-bit decoders and buffering NAND gates to achieve optimal performance. The first NOR plane utilizes dynamic precharge logic with triggered input decoders that AND all inputs with the clock signal. The innovative buffering NAND gate replaces traditional inverter buffers between the two NOR planes, providing automatic precharge of node q and predischARGE of node r during the clock precharge phase. This architecture eliminates ground switches, reduces parasitic capacitances, and prevents racing problems without requiring delayed clock signals.

Figure(a): Low-Power High-Speed Dynamic PLA Circuit Configuration

The circuit demonstrates superior switching characteristics with PMOS ( $W/L = 2.25/0.6$ ) and NMOS ( $W/L = 0.9/0.6$ ) transistor sizing optimized for 0.6 $\mu$ m CMOS technology. The triggered decoder ensures inputs are only active during evaluation phase, while the buffering NAND gate maintains proper logic states and prevents unwanted transitions.

## **IV. PROPOSED SYSTEM:**

The proposed system focuses on the design and implementation of a revolutionary single-clock dynamic PLA architecture using 0.6 $\mu$ m CMOS technology with CADENCE and HSPICE simulation platforms. The architecture strategically combines three essential design elements: triggered one-bit decoders, dynamic NOR planes, and buffering NAND gates. The triggered decoder stage plays a crucial role in conditioning input signals by ANDing them with the clock, ensuring proper timing and reducing power consumption during precharge phases. The dynamic NOR planes implement the core Boolean logic functions while maintaining high-speed operation through optimized transistor networks.

The buffering NAND gate represents the key innovation, simultaneously addressing multiple design challenges including racing problems, ground switch elimination, and power optimization. This structured approach ensures the PLA achieves minimal propagation delay, zero static power dissipation, and superior noise immunity essential for high-performance applications. The design has been extensively evaluated against existing architectures including pseudo-NMOS, traditional NOR-NOR, domino logic, and other advanced PLA configurations to demonstrate significant improvements in power-delay product metrics.

The proposed PLA is exceptionally well-suited for integration into VLSI processor control units, combinational logic circuits, sequential state machines, and complex Boolean function implementations, making it a robust and versatile solution for modern low-power, high-speed digital systems.

## **APPLICATIONS OF LOW-POWER HIGH-SPEED DYNAMIC PLA:**

1. VLSI Processor Control Units – Implements complex control logic for microprocessors, microcontrollers, and DSP cores with optimized power and speed characteristics.
2. Memory Address Decoders – Provides efficient row and column decoding in memory arrays, cache systems, and content-addressable memories.
3. State Machine Implementation – Realizes sequential logic circuits, finite state machines, and protocol controllers in communication systems.
4. Arithmetic Logic Units (ALUs) – Implements Boolean functions and control logic within computational units of processors and digital signal processors.
5. Instruction Decoders – Decodes complex instruction sets in RISC and CISC processors, enabling efficient instruction execution.
6. Error Correction Circuits – Implements syndrome generation and error correction logic in memory systems and communication protocols.
7. Digital Signal Processing – Provides configurable logic functions for adaptive filters, FFT processors, and digital communication systems.
8. System-on-Chip (SoC) Integration – Serves as reconfigurable logic blocks in mixed-signal SoCs and embedded system applications.
9. Communication Protocol Processors – Implements protocol-specific logic in network processors, wireless basebands, and interface controllers.
10. Power Management Systems – Provides decision logic for dynamic voltage scaling, clock gating, and power mode transitions in modern processors.

**CONCLUSION:**

The design and analysis of the low-power high-speed dynamic PLA circuit using single-clock CMOS technology successfully demonstrates its superiority over conventional architectures in achieving optimal power-speed trade-offs. By strategically integrating triggered one-bit decoders, dynamic NOR planes, and innovative buffering NAND gates, the proposed architecture eliminates racing problems, reduces power consumption, and enhances operational speed while maintaining design simplicity. Simulation results validate its exceptional performance with the fastest propagation delays (2.6ns rise, 15.56ns fall) and lowest power-delay product among evaluated designs.

**REFERENCE:**

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