

Design of High Gain and Low Noise CMOS

Gilbert Cell Mixer for Receiver Front End Design

Abstract

This paper presents the design of a low noise CMOS Gilbert cell mixer in 180 nm technology with the help of cadence tool. The switched biasing technique is used to improve the noise performance by splitting the tail current source into two small transistors. The supply voltage required for the circuit is 1.8 V with a power consumption of 3.5 mW. The layout of the present design is also given here. This design results better performance in the conversion gain, noise figure and power consumption than the conventional mixer design available in the literature. Hence, this design is a suitable block for receiver front end design for wireless systems.

Introduction : The radio frequency (RF) integrated circuit has received much more interest due to their linearity, low power, low cost and high level of integration. The RF front end processes the incoming RF signal, before it altered into a lower intermediate signal (IF). As shown in Fig. 1, the conventional receiver front end consists of low-noise amplifier (LNA), mixer, local oscillator (LO), IF amplifier and different filters . RF Mixer is a 3 port active or passive frequency translation device having two inputs and one output port. When RF frequency and LO frequency are inserted into the two input ports, it creates the sum or the difference frequency ($RF \pm LO$), which is called the IF frequency. The most accepted double balanced active mixer in RFIC design is the Gilbert cell mixer. Generally, the Gilbert cell mixers are used as the down converter in RF front end receiver design. This is due to the good conversion gain at wide band, high linearity and good isolation. Of course it requires high supply voltage and consumes more power. From the different advanced technology CMOS mixers found in the literature, it seems that the folded structure mixer works at a low supply voltage due to the small number of stacked transistors. But it requires a higher dc current for the operation. It suffers from large chip area due to the inductor used in the matching network. The bulk driven concept outcomes low supply voltage requirements as number of stacked transistor are less and lower power consumption. However, due to the straight insertion of RF signal through the body terminal, it is noisier. In one hand, the subthreshold technique results low power and high gain by the use of an active load. But in the other hand, it gives more noise to the system due to the high

Circuit Diagram :



Schematic :

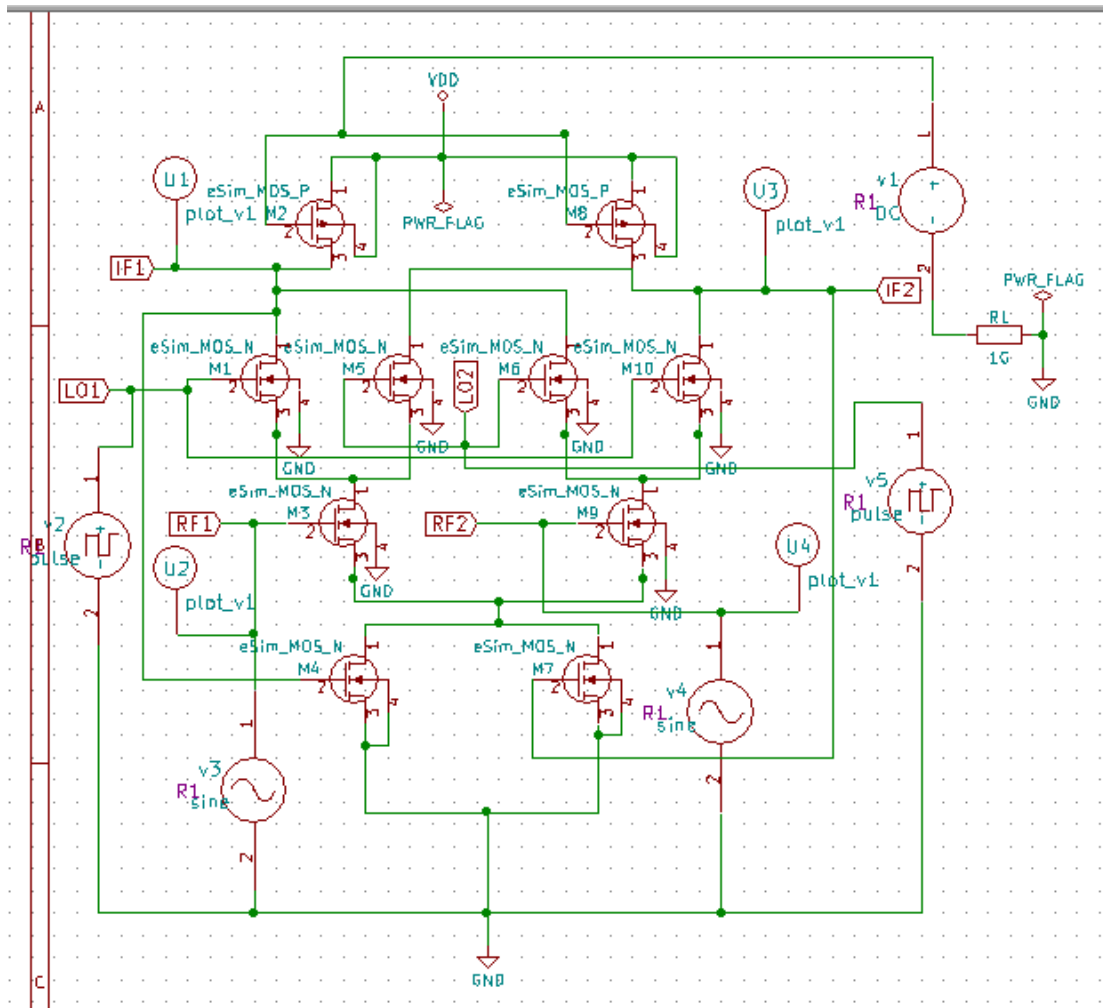


Fig - 2 : Schematic of Gilbert Mixer Cell in Esim

Simulation Results :

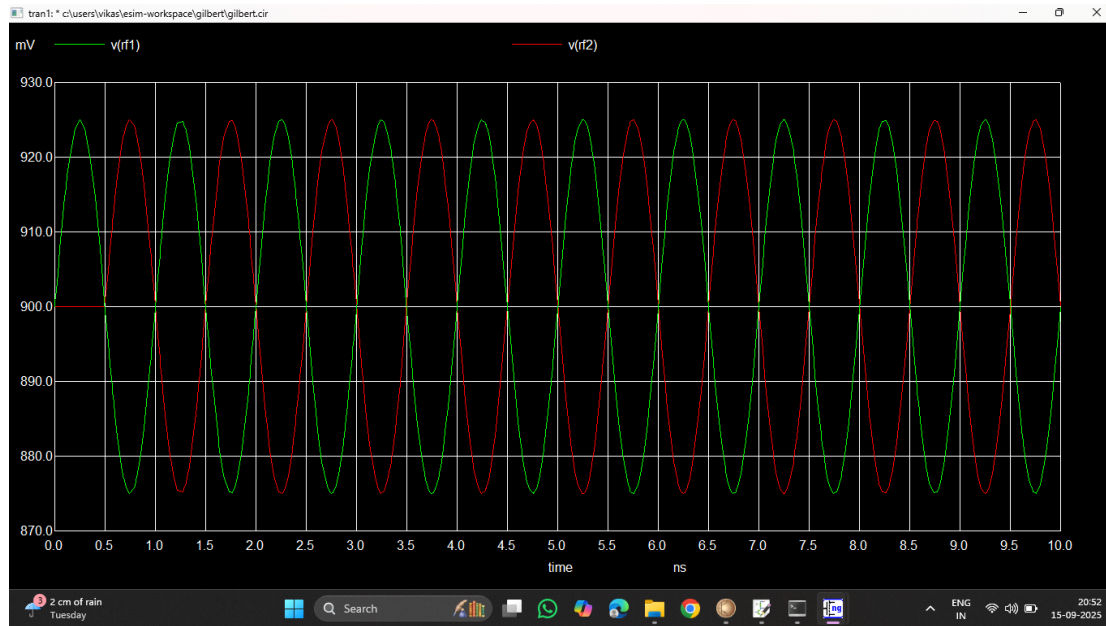


Fig - 3 : Differential Radio Frequency Signal (RF+ / RF-)

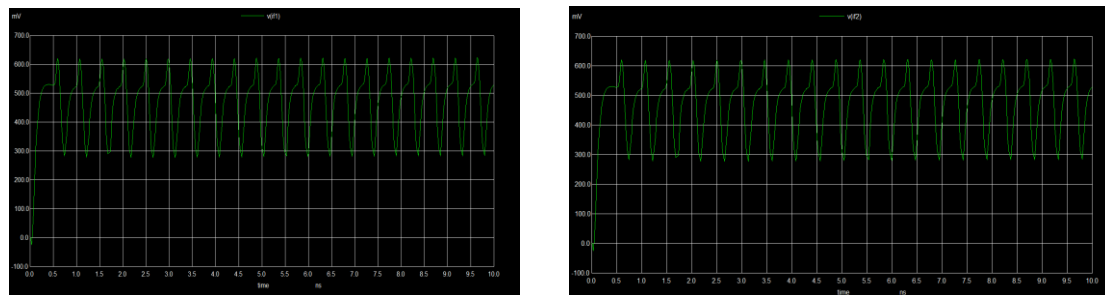


Fig - 4a & 4b : Outputs of Intermediate Frequency Signals (IF+ / IF-)

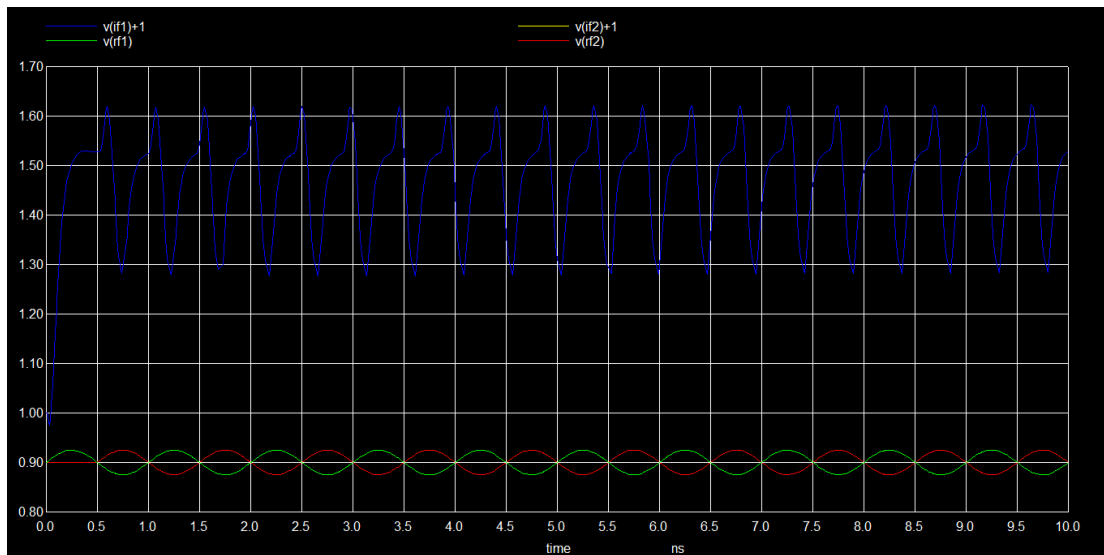


Fig - 5 : Transient Analysis of Mixer

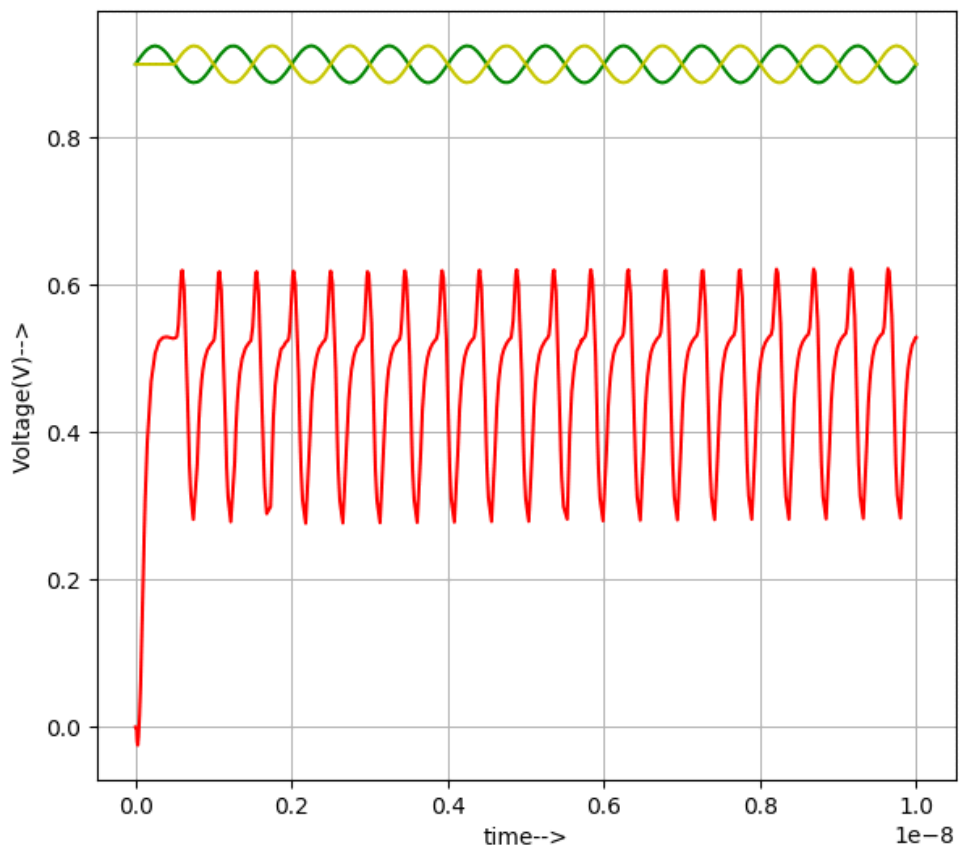


Fig - 6 : Python Plot of Mixer

Conclusion : The design of a low noise CMOS Gilbert cell mixer using switched biasing technique is explained here. The proposed mixer is implemented in 180 nm technology process with the help of cadence tool. The switched biasing technique is used to improve the noise performance. The power consumed by the circuit is 3.5 mW. Also the layout design is presented in this paper. This design results improved performance in the noise figure, power consumption and conversion gain than the conventional mixer design. Hence, this design may be implemented in wideband and multi-standard integration applications.

Reference :

1. Shasanka Sekhar Rout , Kabiraj Sethi, " Design of High Gain and Low Noise CMOS Gilbert Cell Mixer for Receiver Front End Design ", IEEE Conference Paper December 2016. Link - <https://ieeexplore.ieee.org/abstract/document/7966800>
2. F. C. Chang, P. C. Huang, S. F. Chao, and H. Wang, "A low power folded mixer for UWB systems applications in 0.18 μ m CMOS technology," IEEE Microw. Wireless Compon. Lett., vol. 17, no. 5, pp. 367–369, May 2007.
3. K. H. Liang, Y. J. Chan, and H. Y. Chang, "A 0.5-7.5 GHz ultra lowvoltage, low-power mixer using bulk injection method by 0.18 μ m CMOS technology," IEEE Microw. Wireless Compon. Lett., vol. 17, no. 7, pp. 531-533, Jul. 2007.

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