

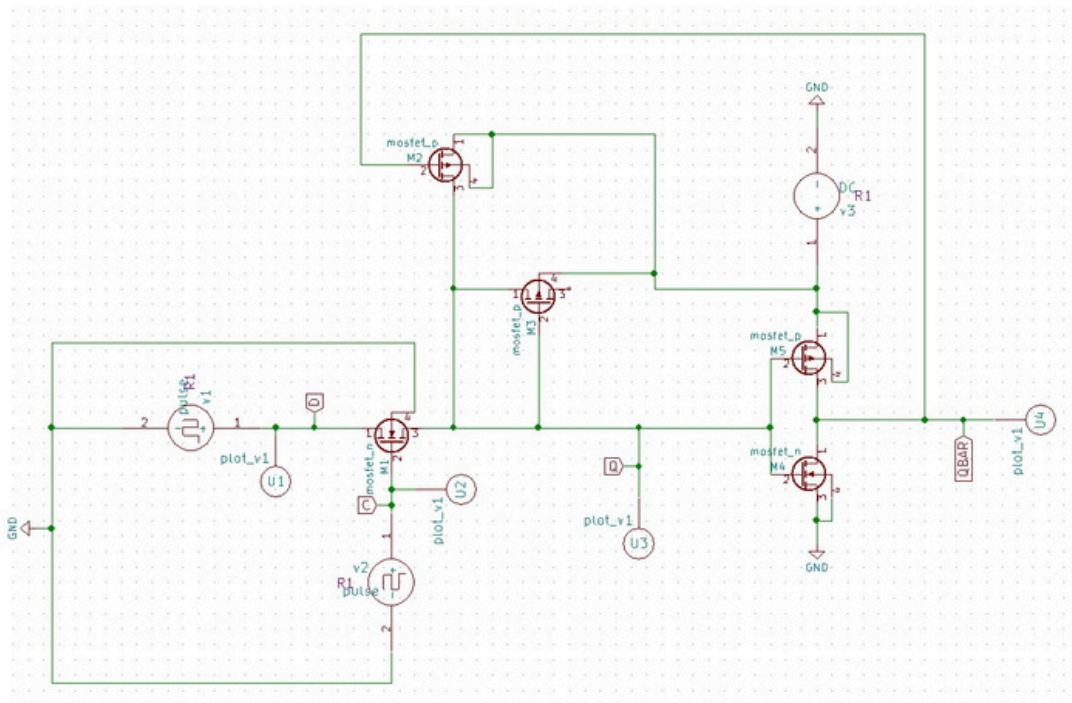
IMPLEMENTATION OF 5-TRANSISTOR (5T) LATCH USING OPTIMIZED TRANSISTOR COUNT IN ESIM

-Santhosh C

Theory/Description:

- The 5T latch stores one bit of digital data by using a feedback loop between transistors, allowing it to latch or hold the output state indefinitely without a continuous input.
- The latch operates by using transistors configured such that when an input signal sets a transistor ON, it triggers a chain reaction, switching states and feeding back to sustain this state until reset.
- Reducing transistor count decreases the chip area required, lowers dynamic and static power consumption, and can improve speed due to fewer transistor switching stages.
- Transistors in the latch switch between cutoff (OFF) and saturation (ON) states, holding either logic 0 or logic 1 output.
- Feedback paths ensure state preservation through cross-coupled transistor connections.

Circuit Diagram:



- The 5-transistor (5T) latch is a digital memory circuit designed to store one bit of information using only 5 transistors, unlike conventional latches that use 6 or more transistors. This reduction makes the circuit simpler, smaller in area, and more power-efficient. It works by using feedback between the transistors to maintain its output state (either 0 or 1) until changed by the input. The design aims to improve performance by reducing delay and power consumption, making it suitable for lowpower VLSI applications. The circuit is simulated at the transistor level using eSim software for accurate analysis and verification. Overall, the 5T latch is an optimized, compact, and efficient alternative to traditional latch designs.

Trurth Table :

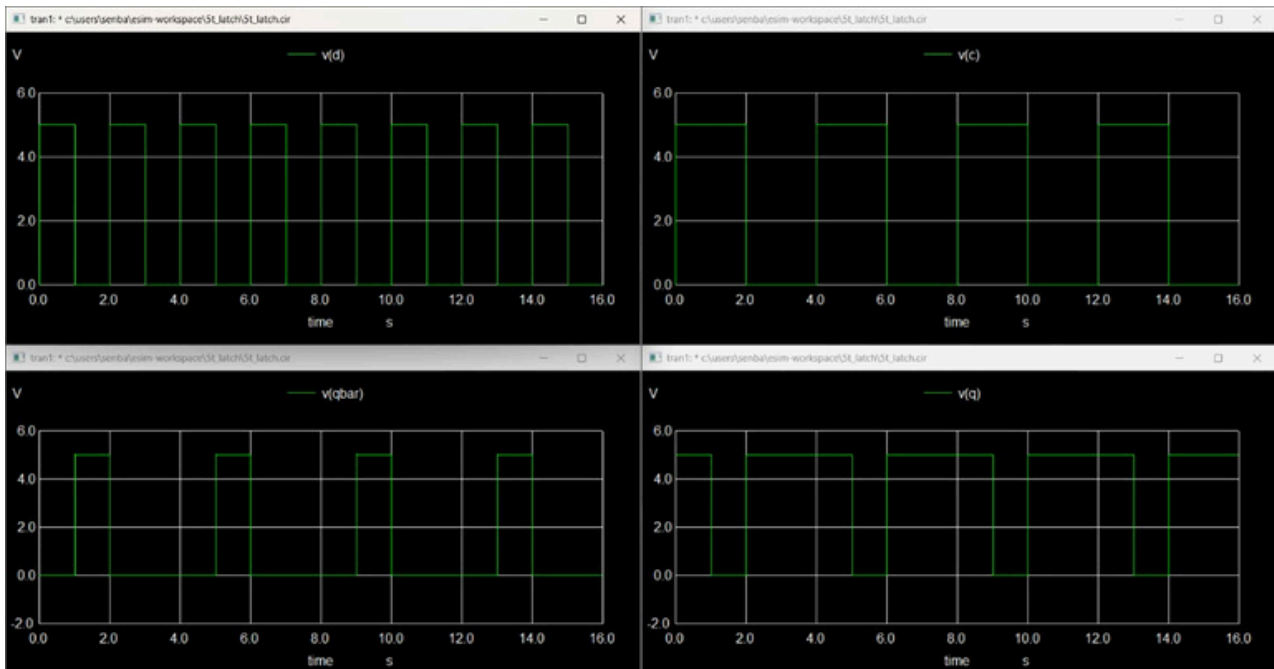
Input Signal (D,C)	Output (Q)	Qbar
00	Hold	Hold
01	0	1
10	1	0

- The latch stores and holds the output Q depending on the inputs, where Q' is always the complement of Q

Result/Output :

- The 5T latch successfully reduces power consumption and area usage compared to traditional 6T designs.
- Outputs remain steady at logic HIGH or LOW corresponding to Set or Reset inputs.
- Resulting output can be used as a memory element or part of sequential circuits in VLSI design.

Output Waveform :



Performance Analysis :

- The 5-transistor (5T) latch is a compact digital memory element designed to reduce the transistor count from the conventional 6 or more to only 5. This reduction lowers chip area, power consumption, and propagation delay, making it suitable for low-power VLSI applications. The circuit maintains stable data storage through transistor feedback loops. It simplifies design by minimizing routing complexity and parasitic effects. Simulation confirms efficient performance and reliability. Overall, the 5T latch is an optimized, power-efficient, and area-saving solution for modern digital circuits

References:

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- C. A. Kumar, B.K. Madhavi, and K. L. Kishore, "Enhanced Clock Gating Technique for Power Optimization in SRAM and Sequential Circuit," *Journal of Automation Mobile Robotics & Intelligent Systems*, pp. 32–38, Jan. 2022.