

Implementation of 4-Bit Ripple Carry Adder Using Optimized 10T Full Adder in eSim

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Theory / Description:

Adders are the fundamental building blocks of arithmetic logic units (ALUs) and play a critical role in digital systems. Among different adder architectures, the Ripple Carry Adder (RCA) is widely used due to its simple structure. However, conventional CMOS-based RCAs suffer from **high transistor count**, larger **chip area**, and increased **power consumption**.

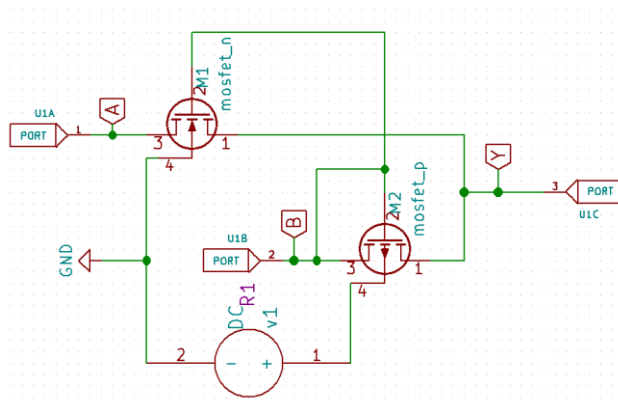
A standard CMOS Full Adder requires **28 transistors**, leading to **112 transistors** for a 4-bit RCA. To address this limitation, an **optimized 10-transistor (10T) Full Adder** is employed to implement the RCA, reducing the overall transistor count to **40**. This reduction in transistor count leads to lower power dissipation, smaller area utilization, and improved performance.

In this work, a **4-bit Ripple Carry Adder using 10T Full Adders** has been designed and simulated using **eSim**. The performance parameters such as functionality, transistor count, and simulation results are analyzed and compared with conventional CMOS RCA designs.

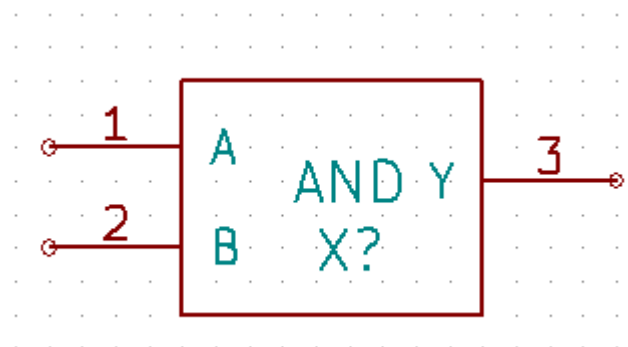
Circuit Diagram(s)

AND Gate:

- The AND gate has been implemented using **Pass Transistor Logic (PTL)**.
- Only **2 transistors** are used to realize the AND function, significantly reducing transistor count compared to CMOS logic.
- The schematic has been designed and the subcircuit created in **eSim** for reuse in higher-level designs.



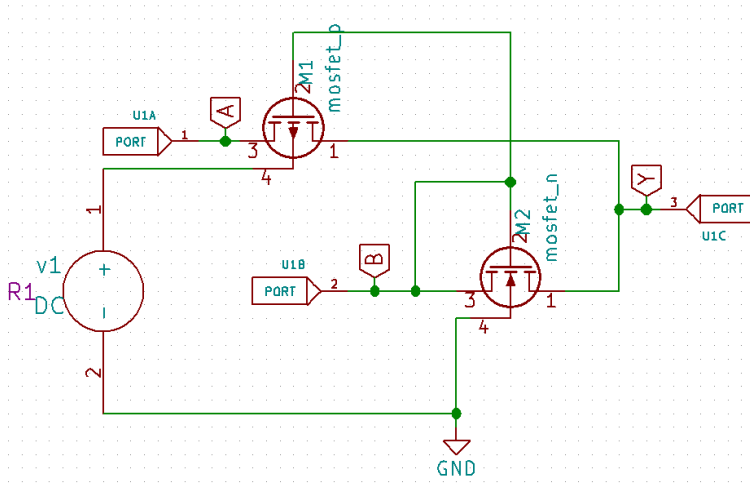
Schematic Diagram of AND gate



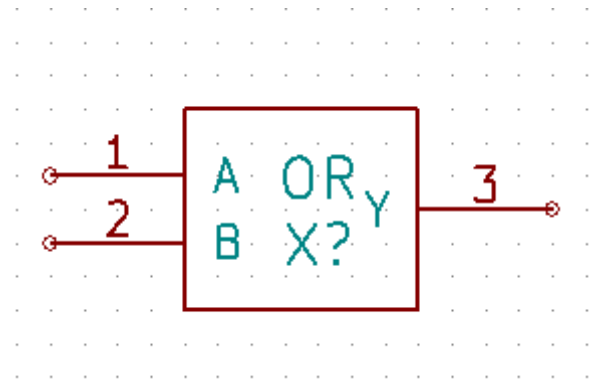
Subcircuit of AND gate

OR Gate:

- The OR gate is also implemented using **Pass Transistor Logic (PTL)**.
- Similar to the AND gate, it requires only **2 transistors**, making it compact and area-efficient.
- The schematic diagram and corresponding subcircuit were created in **eSim**.



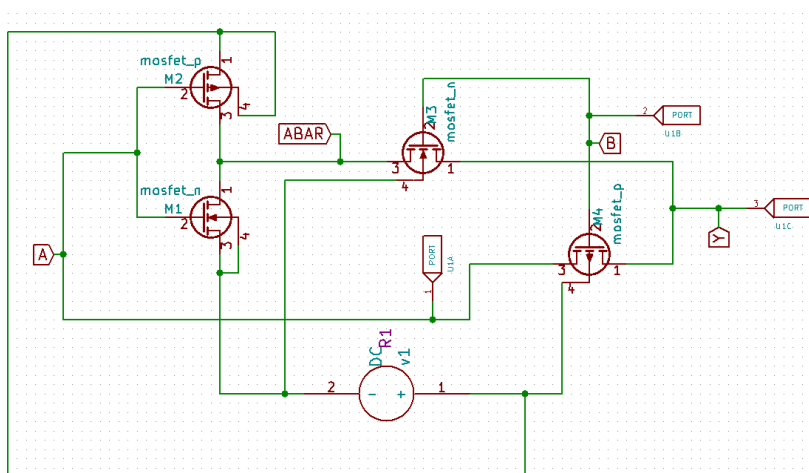
Schematic Diagram of OR gate



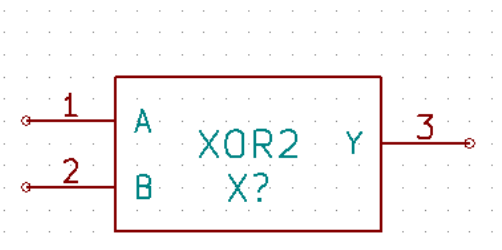
Subcircuit of OR gate

XOR Gate:

- The XOR gate has been designed based on the transistor-level schematic.
- It is realized with **pass-transistor based switching**, which efficiently produces the exclusive OR output.
- The schematic and subcircuit have been created in **eSim** for integration into the Full Adder design.



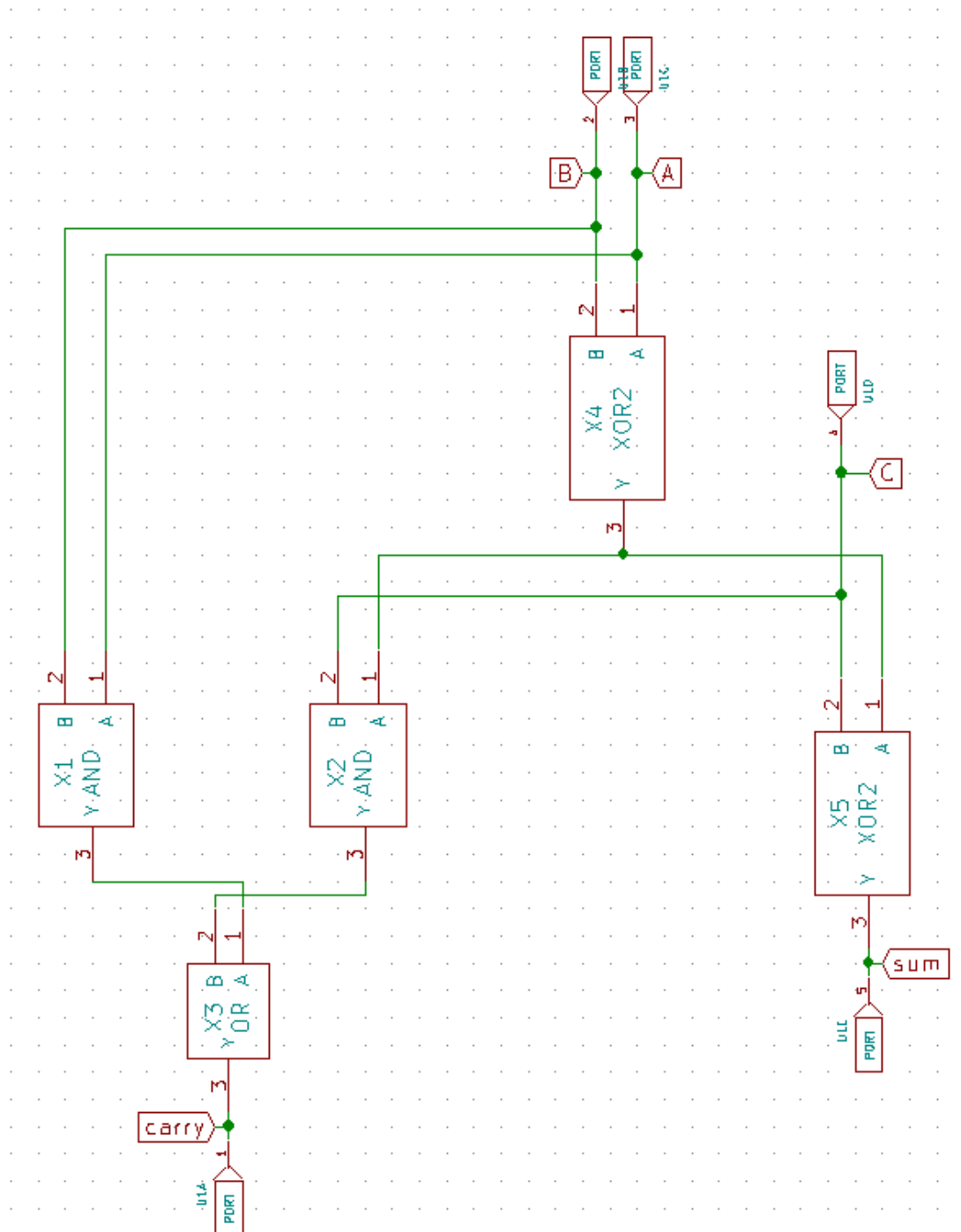
Schematic Diagram of XOR gate



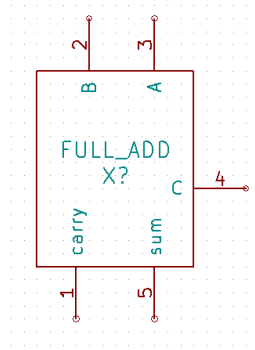
Subcircuit of XOR gate

FULL ADDER:

- The Full Adder is designed using a combination of **2T AND**, **2T OR**, and **optimized XOR gates**.
- The structure requires only **10 transistors**, compared to **28 transistors in conventional CMOS Full Adders**.
- Both **SUM** and **CARRY** outputs are generated, and the subcircuit has been created in **eSim** for cascading in RCA.



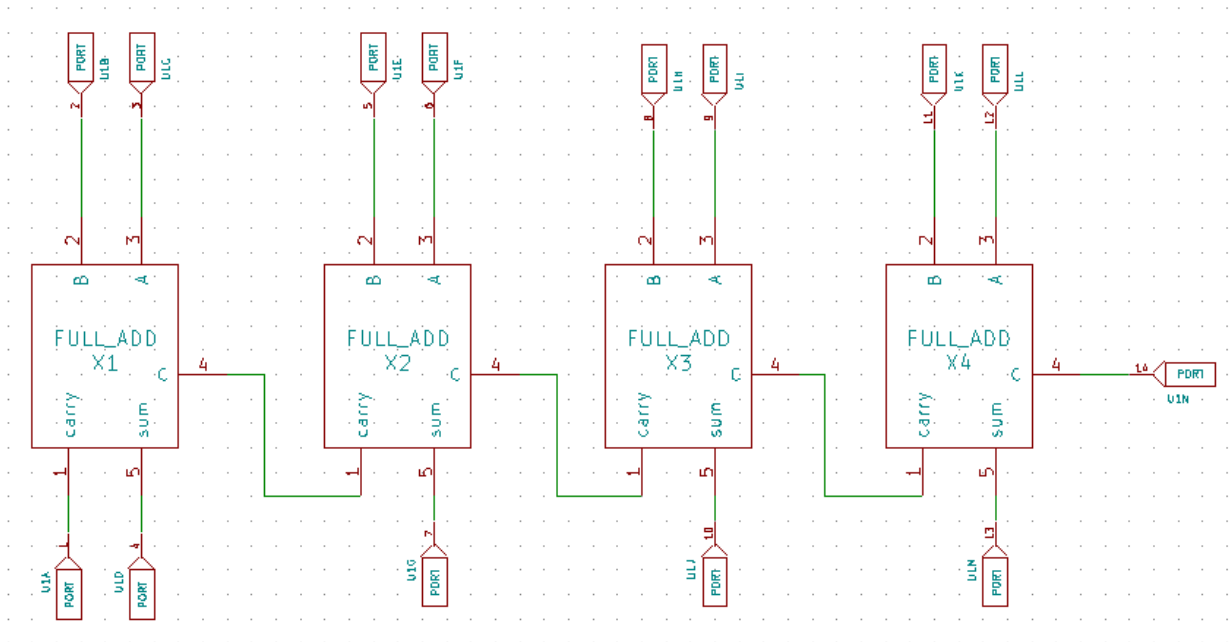
Schematic Diagram of FULL ADDER



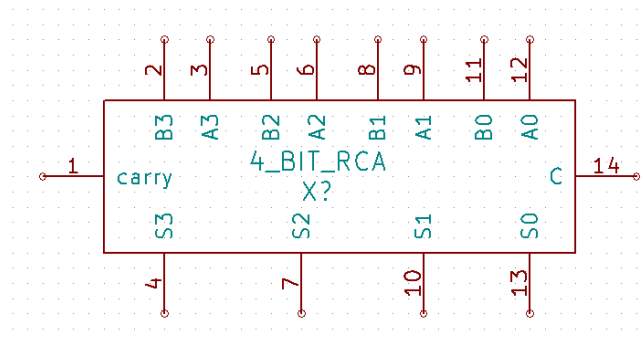
Subcircuit of Full Adder

4-BIR RIPPLE CARRY ADDER:

- The 4-bit RCA is constructed by **cascading four 10T Full Adders**.
- The **carry-out of one stage is connected to the carry-in of the next stage**, creating the ripple effect.
- The schematic was implemented in **eSim**, using the Full Adder subcircuits.



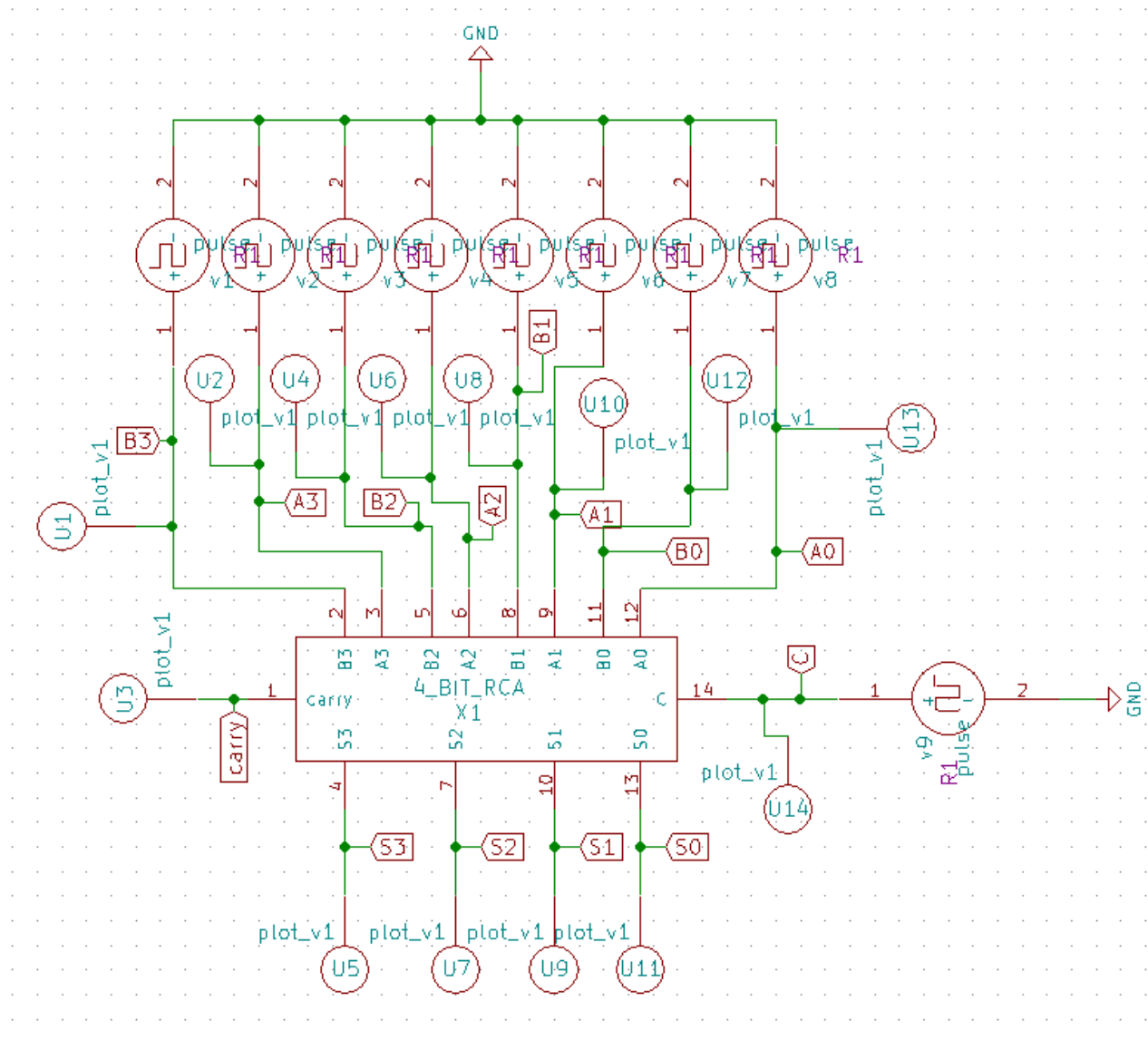
Schematic Diagram of 4-Bit RCA



Subcircuit of 4-Bit RCA

4-BIT RCA TEST CIRCUIT:

- A **testbench circuit** was created in eSim to verify the functionality of the 4-bit RCA.
- Input vectors were applied, and the corresponding **SUM** and **CARRY** outputs were observed through **ngspice simulations**.
- This verified the correctness of the proposed 10T RCA design



4 Bit RCA test circuit

TRUTH TABLE:

INPUT				OUTPUT			
A1	A0	B1	B0	C _{OUT}	S2	S1	S0
0	0	0	0	0	0	0	0
0	0	0	1	0	0	0	0
0	0	1	0	0	0	0	0
0	0	1	1	0	0	0	0
0	1	0	0	0	0	0	0
0	1	0	1	0	0	0	1
0	1	1	0	0	0	1	0
0	1	1	1	0	0	1	1
1	0	0	0	0	0	0	0
1	0	0	1	0	0	1	0
1	0	1	0	0	1	0	0
1	0	1	1	0	1	1	0
1	1	0	0	0	0	0	0
1	1	0	1	0	0	1	1
1	1	1	0	0	1	1	0
1	1	1	1	1	0	0	1

4-Bit RCA Truth Table

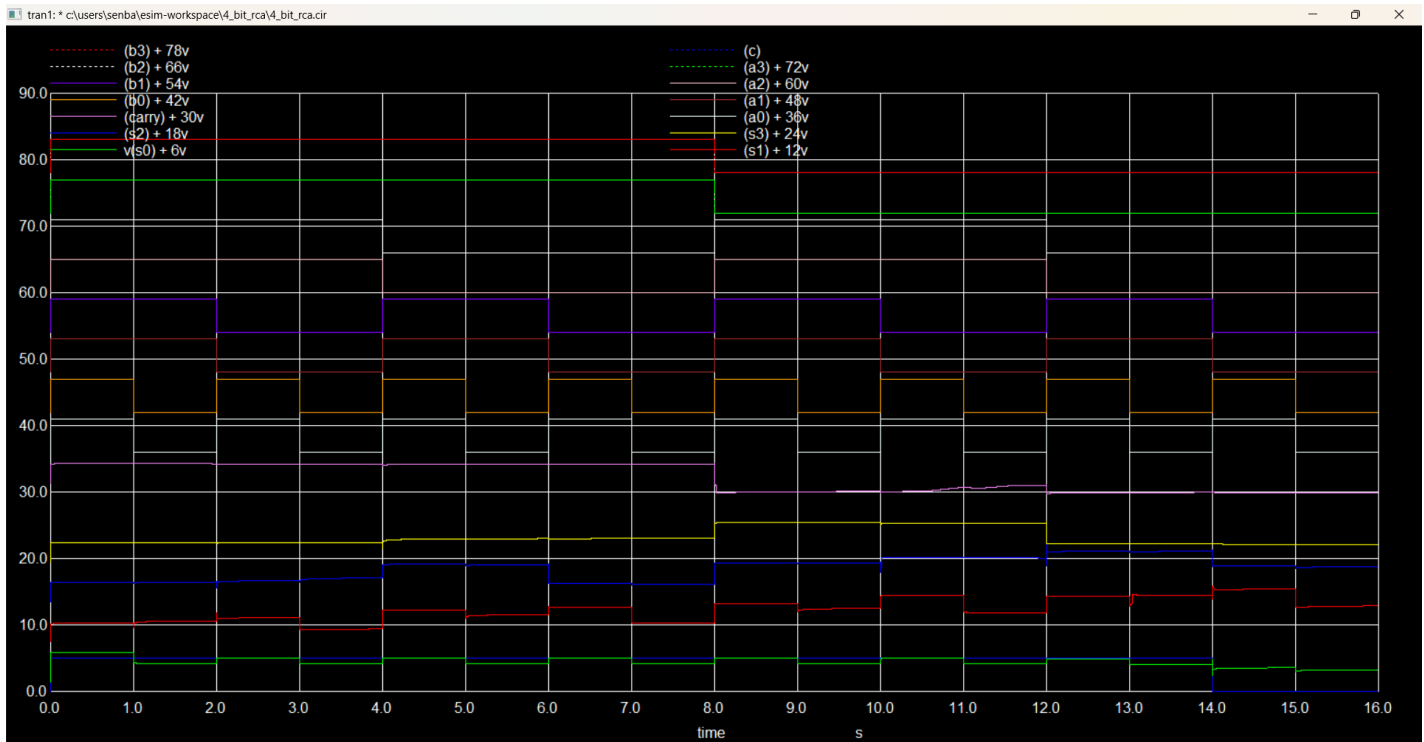
RESULTS / OUTPUT:

- **ngspice Simulation:**

The designed 4-bit Ripple Carry Adder was simulated using **ngspice** in eSim. The simulation verified the **SUM** and **CARRY outputs** for all possible input combinations, confirming correct logical behavior.

- **Waveform Verification:**

The **stacked transient output waveform** clearly shows the correct generation of **SUM (S0–S3)** and **CARRY outputs** with respect to different input combinations. This validates the functionality of the **10T Full Adder based 4-bit RCA**.



4 Bit RCA Output Planner

- **Performance Analysis:**

- The proposed 10T design reduces the **transistor count** from **112 (conventional CMOS RCA)** to **40 (10T RCA)**.
- Due to fewer transistors, the design shows **lower area utilization** and **reduced power dissipation**, making it more efficient for VLSI applications.
- Propagation delay is also reduced since the carry logic is optimized with pass-transistor structures.

REFERENCES:

1. *Design, Simulation and Comparative Analysis of CMOS Ripple Carry Adder*, **International Journal of Research in Electronics and Computer Engineering (IJRECE)**, Vol. 6, Issue 2, Apr.–June 2018, ISSN: 2393-9028 (Print) | 2348-2281 (Online).
2. S. Goel, A. Kumar, and M. A. Bayoumi, “*Design of robust, energy-efficient full adders for deep-submicrometer design using hybrid-CMOS logic style*,” **IEEE Transactions on VLSI Systems**, vol. 14, no. 12, pp. 1309–1321, Dec. 2006.
3. S. Wairya, R. K. Nagaria, and S. Tiwari, “*New design methodologies for high speed low power 1-bit CMOS full adder circuits*,” **International Journal of VLSI Design & Communication Systems (VLSICS)**, vol. 2, no. 3, pp. 47–59, Sept. 2011.
4. A. Shams and M. Bayoumi, “*A novel high-performance CMOS 1-bit full-adder cell*,” **IEEE Transactions on Circuits and Systems II: Analog and Digital Signal Processing**, vol. 47, no. 5, pp. 478–481, May 2000.