Simulation of Six-Stage Linear CMOS Charge Pump with Complementary Clocking

Pravin A
Dept of Electronics and Communication Engineering
Sri Eshwar College of Engineering, Coimbatore

Abstract

This project presents the design and simulation of a six-stage CMOS charge pump circuit aimed at efficient voltage boosting without the use of inductors. The circuit leverages complementary PMOS and NMOS transistors controlled by non-overlapping clock signals to maximize charge transfer and minimize voltage ripple. The multistage configuration allows progressive voltage multiplication, making it suitable for low-power, integrated applications demanding compact size and high efficiency. The circuit's operation and performance are validated through transient simulation, demonstrating steady and boosted output voltages. This design contributes a practical and scalable architecture for on-chip voltage generation in portable electronic devices.

Keywords: CMOS charge pump, multi-stage, voltage multiplier, low-power circuit, voltage boosting

I. INTRODUCTION

Charge pumps are essential circuits used for converting lower DC voltages to higher DC output voltages without inductors, making them suitable for compact and portable electronics. This project focuses on designing a six-stage CMOS charge pump using complementary PMOS and NMOS transistors. The circuit employs non-overlapping clock phases to optimize charge transfer efficiency and reduce voltage ripple. The resulting design offers an efficient, scalable voltage booster compatible with modern CMOS technology and low-power applications.

II. PURPOSE OF SIX-STAGE CMOS CHARGE PUMP

The six-stage CMOS charge pump is designed to generate higher output voltages from a lower DC input without using inductors. It efficiently boosts voltage through the staged transfer of charge using complementary PMOS and NMOS switches. The circuit aims to provide low ripple and high voltage gain suitable for integrated and portable electronics. It ensures high power conversion efficiency by employing non-overlapping clock signals. The multistage approach allows progressive voltage multiplication while reducing voltage drop losses. This design is particularly useful in low-power applications requiring compact, on-chip voltage regulation. The charge pump can be integrated with systems like phase-locked loops, EEPROM programming, and display drivers.

III. WORKING PRINCIPLE

The Cross-Coupled Charge Pump operates by transferring charge through complementary pairs of MOSFET switches and capacitors driven by two non-overlapping clock signals. These clocks alternately drive the gates of NMOS and PMOS transistors in cascaded stages.When first clock goes high, one set of transistors turns on,allowing the first stage capacitor to charge.

1) When the first clock goes high, one set of transistors turns on, allowing the respective capacitor to charge from the supply voltage.
2) When the clock switches low, the stored charge is transferred forward to the next stage through the activated complementary MOSFETs.
3) Simultaneously, the second clock drives the complementary transistor pair, charging the next capacitor and continuing the sequential charge transfer.
4) This alternating sequence progresses through all stages, resulting in a stepwise increase of the output voltage at each stage.
5) The latch-like transfer via cross-coupled transistor pairs reduces threshold voltage drop losses compared to diode-based charge pumps, enhancing efficiency.
6) Ultimately, the output voltage is boosted far beyond the input voltage levels, producing a stable and efficient DC output suitable for low-voltage power applications.

IV. CIRCUIT DIAGRAM

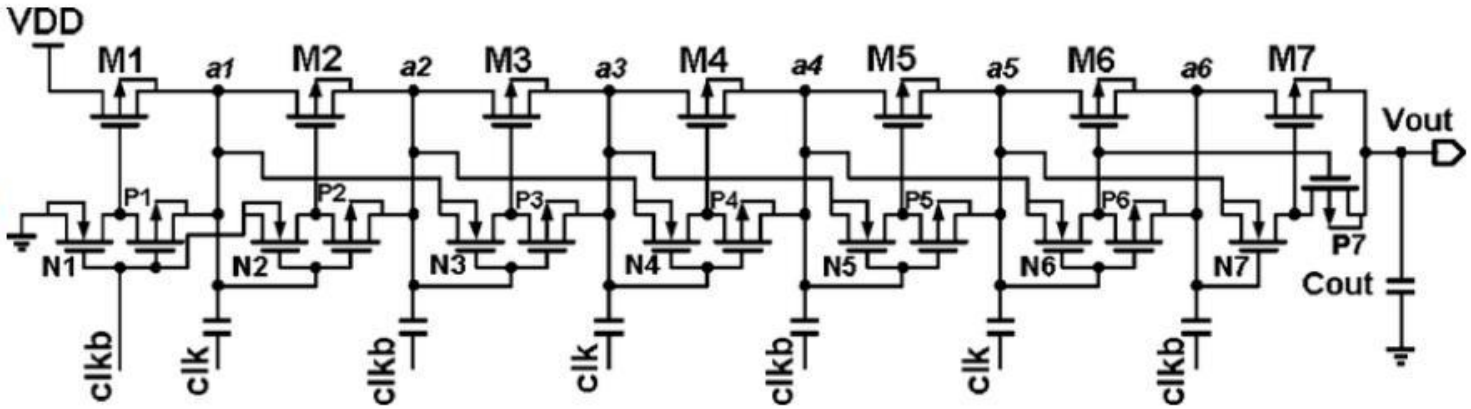

Fig. 1: Six-Stage cmos charge pump circuit diagram

Fig. 1: This is a six-stage linear CMOS charge pump circuit using both NMOS and PMOS transistors arranged in cascaded stages. Alternating clock signals (clk and clkb) control the switches, transferring charge progressively from each stage's capacitor to the next. The multistage design boosts the input voltage by sequentially charging and transferring through the capacitors. The final output, Vout, provides a higher, regulated DC voltage suitable for on-chip power applications.

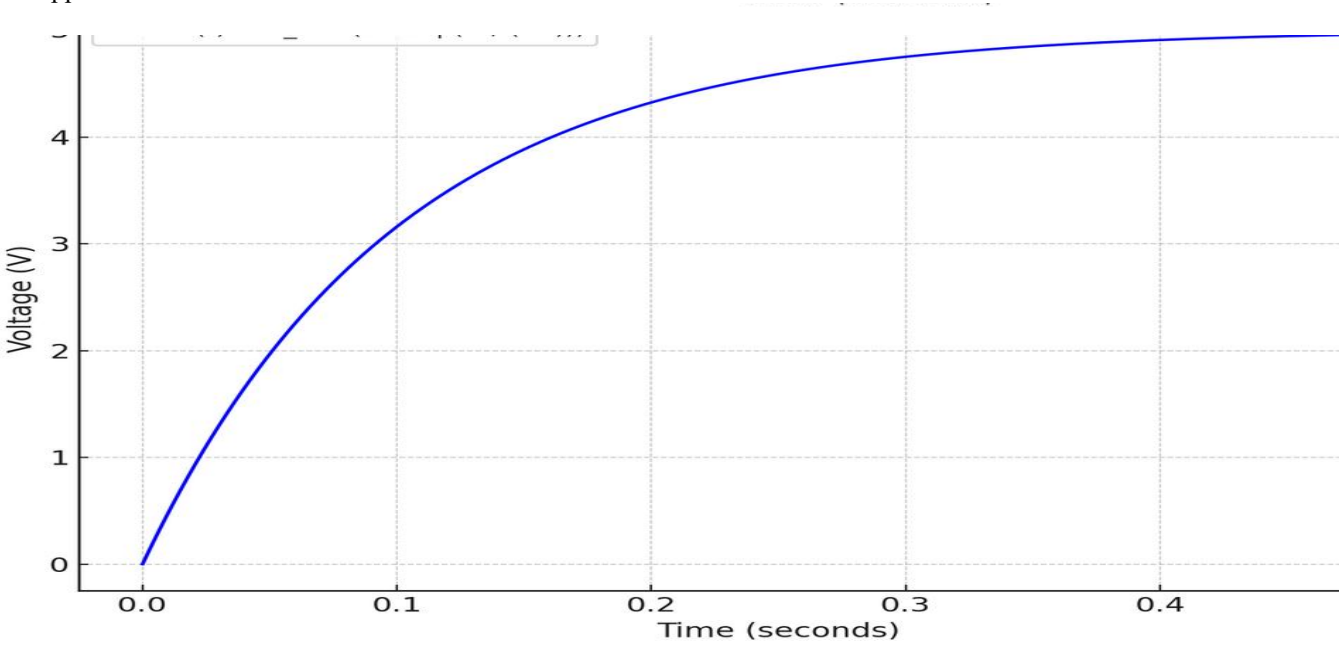

Fig. 2: Six-Stage cmos charge pump output waveform diagram

Fig. 2: The simulation output demonstrates the expected voltage boosting behavior of the CMOS charge pump circuit. The output voltage starts at zero, rises rapidly, and gradually approaches its steady-state value as charge is transferred through the stages. This curve confirms efficient stage-by-stage voltage multiplication and successful circuit operation.

V. Proposed System

The proposed system is a six-stage CMOS charge pump designed to efficiently boost a low input voltage to a higher output voltage using complementary PMOS and NMOS switches. Each stage consists of capacitors and transistor pairs controlled by non-overlapping clock signals for sequential charge transfer. The alternating clock phases enable charging of capacitors and forward transfer of stored charge to subsequent stages. This multistage configuration amplifies the input voltage progressively, increasing output voltage in steps. Cross-coupled transistor pairs help reduce voltage drops caused by transistor thresholds, improving overall efficiency. The design minimizes ripple and power consumption, making it suitable for integrated low-power applications. Simulation and analysis confirm the system's ability to achieve stable, boosted output voltage for on-chip power supply uses.

eSIM CIRCUIT

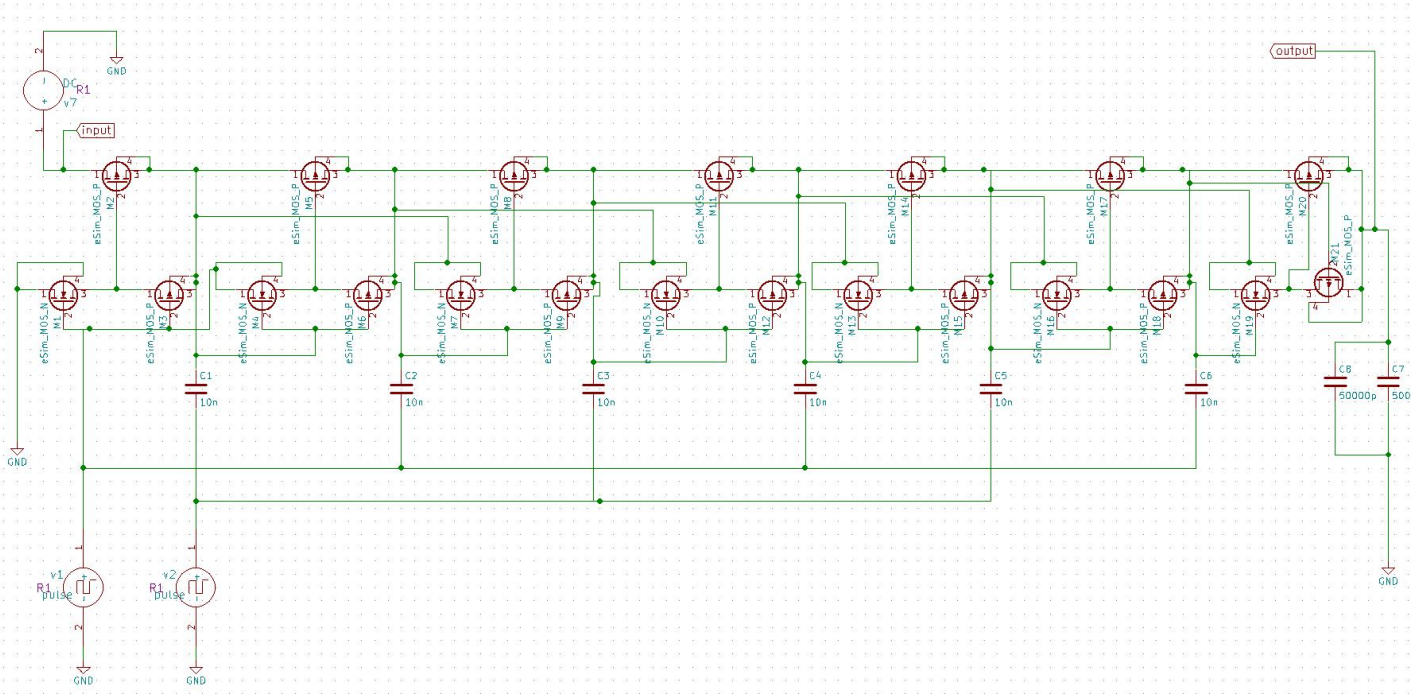

Fig. 3: Cross-Coupled Charge Pump Circuit in eSim

Fig. 3: This is a six-stage CMOS charge pump circuit designed to boost a low input voltage to a higher output voltage in steps. Each stage uses NMOS and PMOS transistors along with capacitors, controlled by two complementary pulse signals for efficient charge transfer. The clock pulses alternately charge and shift energy through the chain of capacitors, progressively increasing the output. The cross-coupled configuration minimizes voltage loss associated with transistor thresholds, enhancing efficiency. The circuit is ideal for on-chip voltage multiplication in low-power electronic systems.

OUTPUT WAVEFORM

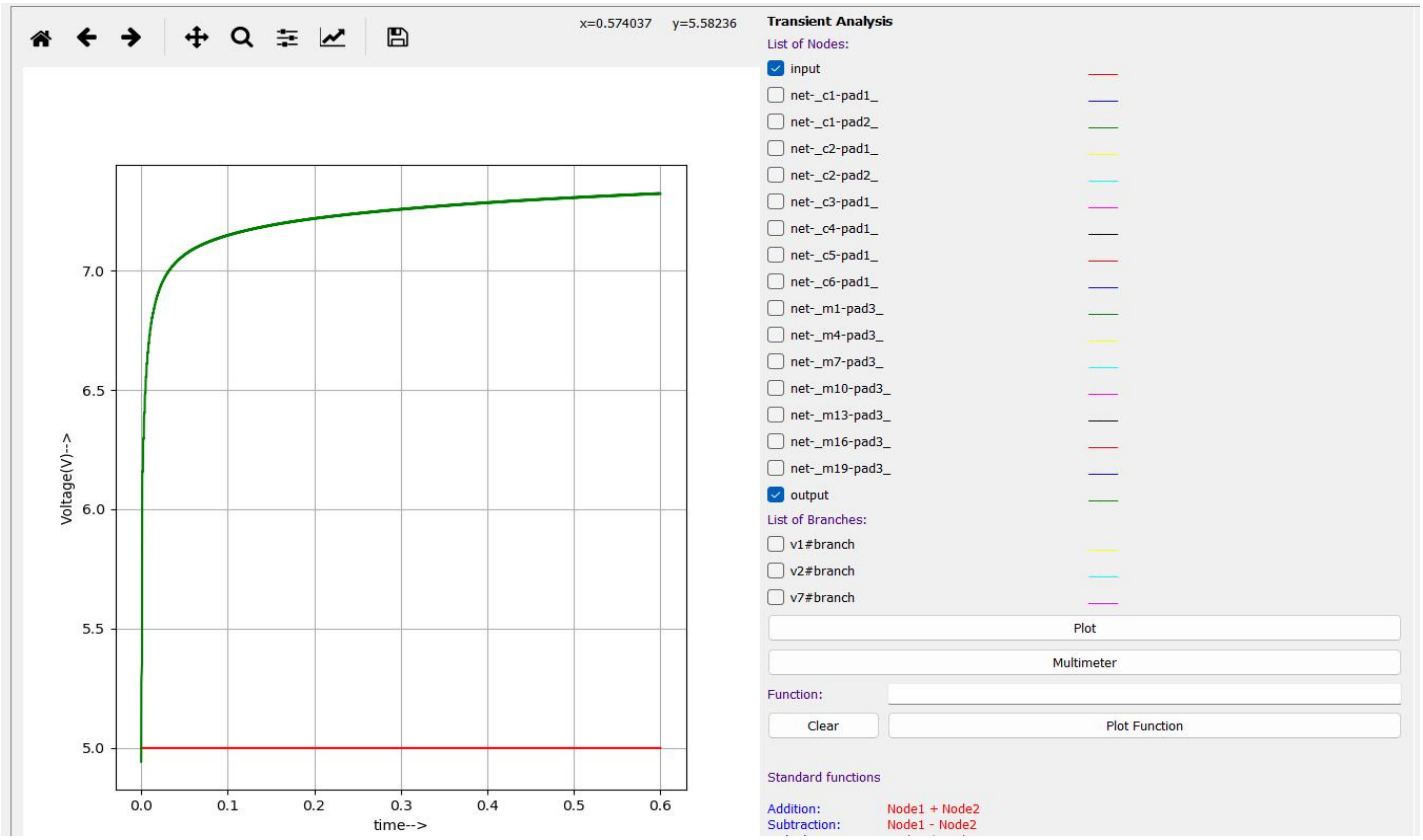

Fig. 4: Output Cross-Coupled Charge Pump Circuit in eSim

Fig. 4: The simulation output shows the output voltage (green curve) rising above the input voltage (red curve) and settling near a steady value over time. This indicates successful voltage boosting by the six-stage CMOS charge pump circuit. The output stabilizes with minimal ripple, demonstrating efficient multi-stage charge transfer and good design. The flat input voltage confirms a constant supply while the boosted output validates proper circuit operation.

V. CONCLUSION

The designed six-stage CMOS charge pump successfully boosts low input voltage to higher stable output levels through sequential charge transfer. Utilization of complementary PMOS and NMOS switches with non-overlapping clocks reduces voltage loss and enhances efficiency. The multistage architecture allows progressive voltage amplification while minimizing ripple and power dissipation. Simulation results confirm the charge pump's effectiveness in delivering boosted and steady output voltage suitable for integrated low-power applications. The design is scalable and adaptable for various on-chip power management needs. Overall, this project demonstrates a practical and efficient approach to on-chip voltage multiplication without inductors.

VII. REFERENCE

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