# Ternary Decoder Using CMOS DPL Binary Gates using esim

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**Abstract**

Ternary logic, as a branch of multi-valued logic (MVL), has emerged as a promising alternative to traditional binary logic due to its ability to represent more information with fewer interconnections, thereby enhancing circuit efficiency and scalability. This paper presents a novel implementation of a ternary decoder using CMOS Double Pass Logic (DPL) binary gates, designed to achieve high performance while maintaining compatibility with conventional CMOS technology. The proposed ternary decoder architecture consists of carefully structured logic stages that effectively generate the required ternary outputs while minimizing power consumption and delay. By exploiting the characteristics of DPL, the design reduces transistor count and interconnection complexity compared to conventional methods, leading to improvements in both speed and energy efficiency. To evaluate the effectiveness of the design, simulations were performed and performance was analyzed in terms of propagation delay, power dissipation, and circuit complexity. Furthermore, the proposed ternary decoder is compared with conventional binary decoder architectures and other multi-valued logic designs to highlight the advantages of the approach. The results demonstrate that ternary logic, when implemented with CMOS DPL, provides a practical foundation for building higher-order MVL circuits such as ternary adders, multiplexers, memory elements, and arithmetic modules. This study emphasizes the potential of ternary logic in advancing VLSI design by offering a balance between performance, area efficiency, and power consumption, making it a valuable reference for future developments in digital and mixed-signal systems.

## I. INTRODUCTION

Decoders are fundamental components in digital systems, responsible for translating coded inputs into unique output signals that drive memory elements, arithmetic units, and other functional blocks. While binary decoders dominate conventional circuit design, the rapid growth of data-intensive applications and the need for more compact, energy-efficient architectures have encouraged exploration beyond traditional two-state logic. Ternary logic, a form of multi-valued logic (MVL), introduces three distinct logic states, thereby increasing information density and reducing the number of interconnections required in a circuit. This makes ternary decoders a promising alternative for improving performance, area efficiency, and scalability in Very Large Scale Integration (VLSI) systems.With continuous advancements in CMOS technology, the design of ternary logic circuits has gained significant attention due to the simultaneous demand for reduced power consumption, higher operating speed, and enhanced circuit reliability. Traditional binary decoder architectures, though simple and well established, face limitations in scalability and efficiency when adapted for MVL applications. To overcome these challenges, novel implementations that exploit circuit-level innovations are required. CMOS Double Pass Logic (DPL) has emerged as a suitable approach, offering advantages in terms of low power, reduced transistor count, and improved switching characteristics.This paper focuses on the design and implementation of a ternary decoder using CMOS DPL binary gates. The proposed design is structured to minimize complexity while generating accurate ternary outputs and ensuring compatibility with existing CMOS processes. In addition, the decoder is evaluated against conventional binary designs and other MVL approaches to highlight the trade-offs involved in terms of speed, power, and circuit area. Such comparative analysis is essential in identifying the most effective architecture for integration into future digital and mixed-signal systems. By providing a detailed study of the ternary decoder, this work aims to serve as a foundation for building more complex MVL circuits, including ternary adders, multiplexers, memory modules, and arithmetic units, thereby contributing to the advancement of high-performance VLSI technologies.

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### PURPOSE OF TERNARY DECODER

The purpose of a ternary decoder circuit is:
The primary purpose of a ternary decoder is to translate multi-valued logic inputs into unique output signals, thereby extending the concept of binary decoding into three logic levels. By supporting states 0, 1, and 2, the ternary decoder increases information density, reduces circuit interconnections, and provides an efficient foundation for building advanced multi-valued logic systems such as ternary adders, multiplexers, and memory units.When implemented using CMOS Double Pass Logic (DPL), the ternary decoder also achieves improvements in speed, power efficiency, and hardware simplicity compared to traditional designs. This makes it highly suitable for modern VLSI applications, where compact layout, low power consumption, and high performance are essential design goals.

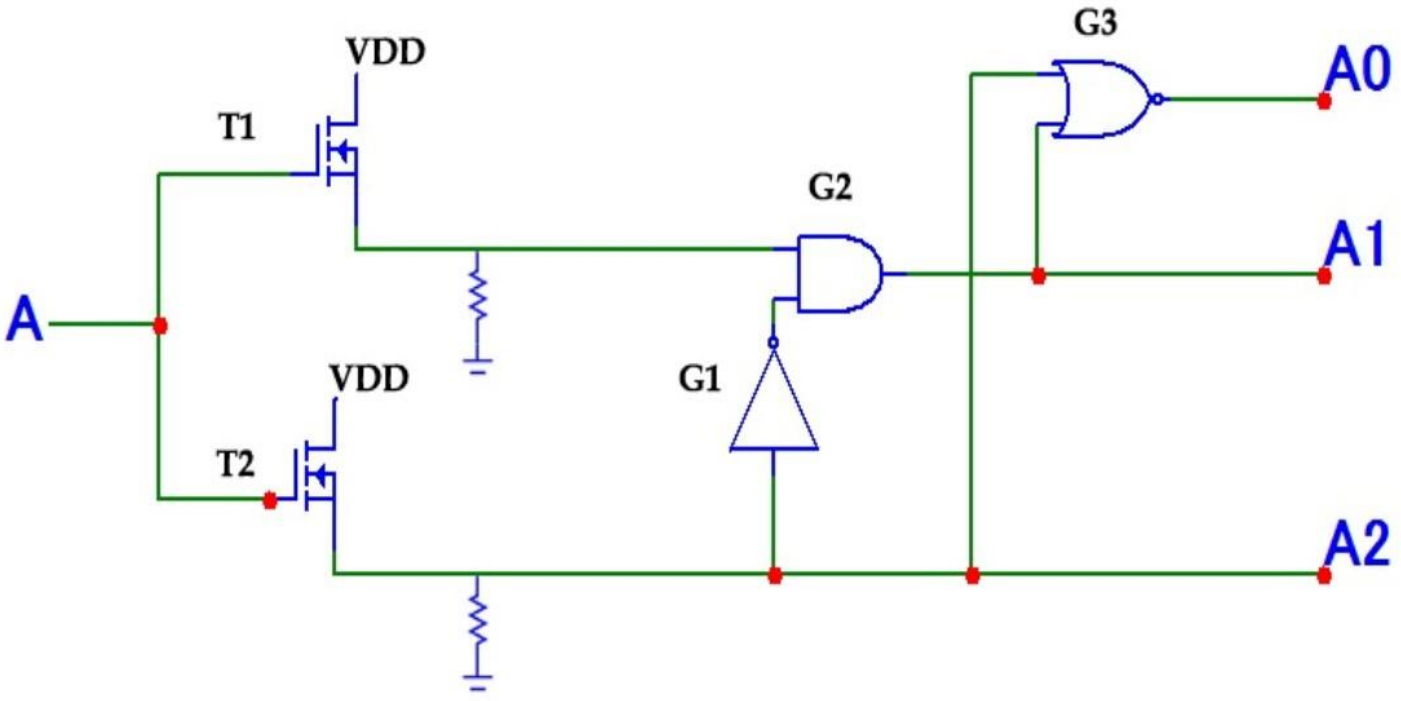
- **Input-to-Output Mapping** – Converts coded ternary input signals into unique output lines, enabling the selection or activation of specific circuit paths.
- **Multi-Valued Logic Operation** – Extends binary decoding to three logic levels (0, 1, 2), increasing information density per input line.
- **Reduced Interconnections** – Minimizes the number of required interconnections in complex circuits, improving scalability and area efficiency.
- **Foundation for MVL Systems** – Serves as a key building block for higher-order ternary circuits such as adders, multiplexers, and memory elements.
- **Efficient VLSI Integration** – Provides faster operation, lower power consumption, and reduced hardware complexity when implemented using CMOS Double Pass Logic (DPL).

**Working Principle**

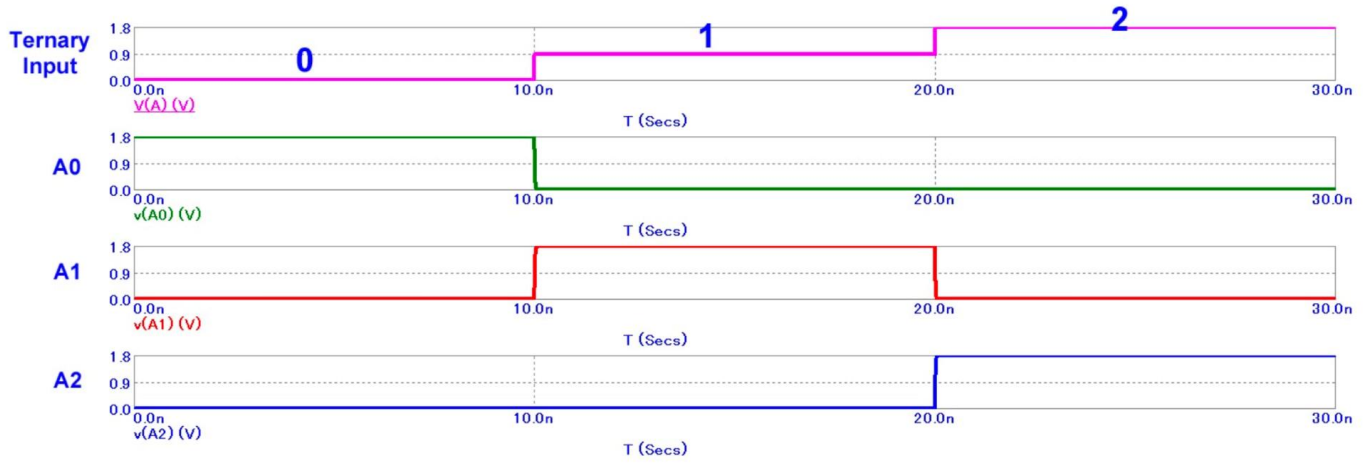
The working principle of a ternary decoder is based on decoding multi-valued logic inputs into a set of unique outputs by using CMOS Double Pass Logic (DPL) gates. Unlike binary decoders, which operate on two input states (0 and 1), a ternary decoder processes three input states (0, 1, and 2) to produce distinct output lines. The key steps in its operation are:

- **Input Application:** The ternary input signals are applied to the decoder, where each input can assume one of three logic states: low (0), medium (1), or high (2)
- **Logic Level Identification:** CMOS DPL gates are used to detect and differentiate between the three input levels, ensuring precise recognition of the applied ternary values.
- **Output Activation:** For each unique combination of ternary input states, a single corresponding output line is activated while all others remain inactive.
- **Signal Integrity and Speed:** The use of DPL reduces signal degradation and ensures fast propagation, maintaining reliable switching between the three levels.
- **Power and Area Efficiency:** Compared to binary decoding of equivalent data, the ternary decoder requires fewer interconnections and transistors, thereby saving power and chip area.
- **Scalability:** This principle can be extended to design larger ternary systems, supporting the development of complex MVL circuits such as memory modules, multiplexers, and arithmetic logic units.
- **Applications:** Ternary decoders are particularly useful in VLSI systems where high performance, reduced complexity, and efficient resource utilization are critical.

**CIRCUIT DIAGRAM**




**Figure(a)**



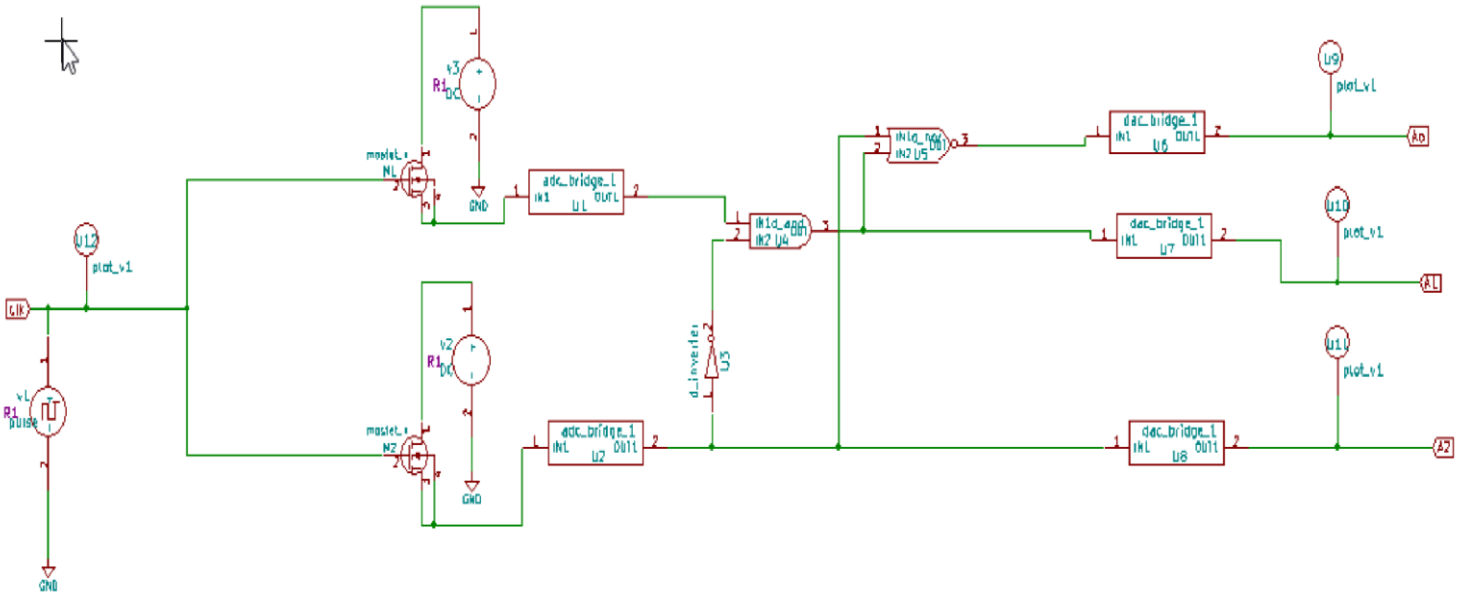

**Figure(b)**

**Fig.a: Circuit of Ternary Decoder**

## II. PROPOSED SYSTEM

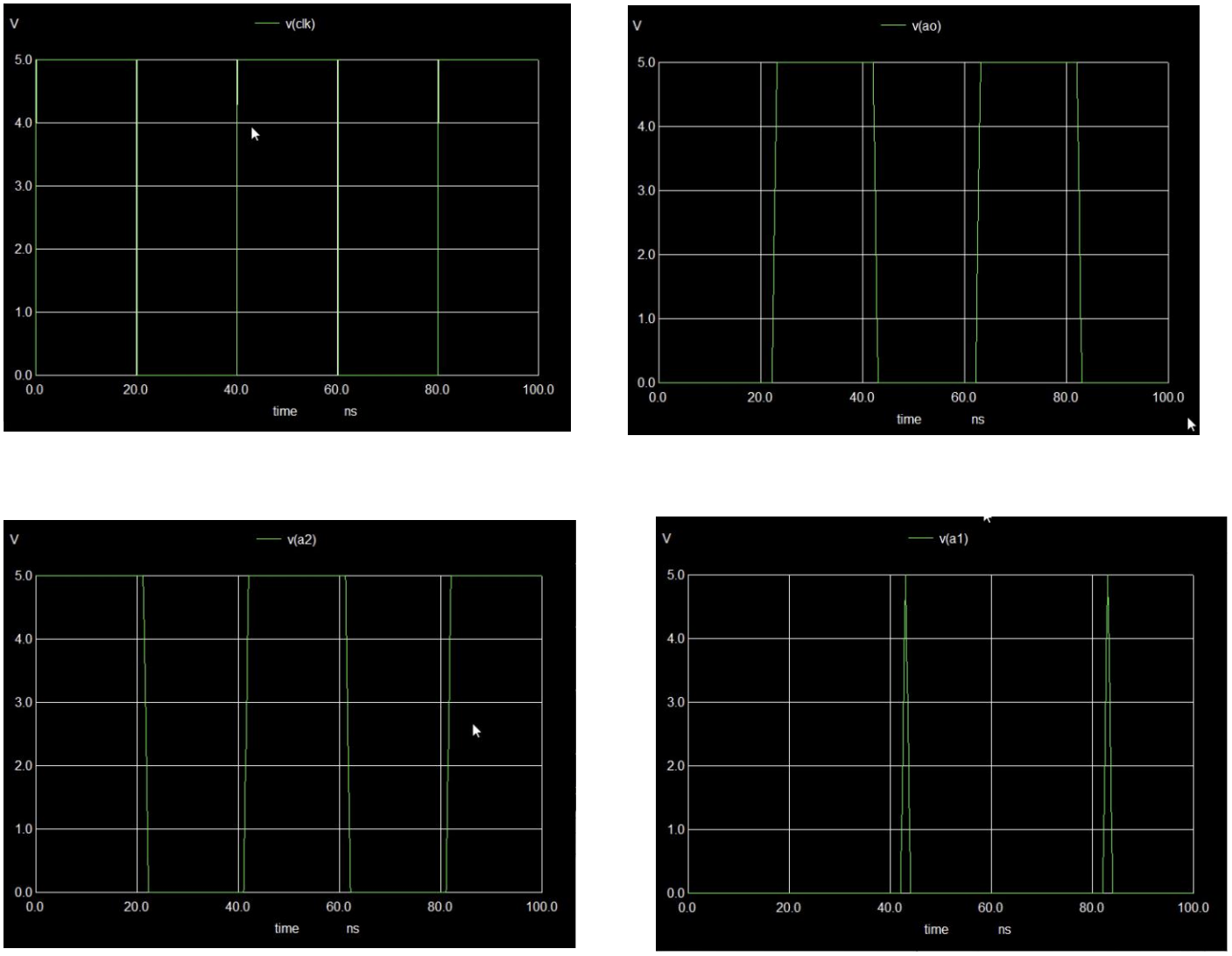
The proposed system focuses on the design and implementation of a ternary decoder using CMOS Double Pass Logic (DPL) technology. The architecture is structured to decode multi-valued inputs, where each input can assume one of three logic states (0, 1, or 2), and generate corresponding unique output lines. By employing DPL-based binary gates, the design minimizes transistor count, reduces interconnection complexity, and ensures reliable detection of ternary input levels. The decoder circuitry effectively distinguishes between the three logic states and activates the appropriate output while keeping others inactive, thereby demonstrating the principle of multi-valued logic in a practical implementation. This structured approach not only improves area efficiency but also achieves low power consumption and faster response times compared to conventional binary decoders. In addition, the system has been analyzed and compared with traditional binary and other MVL designs to highlight trade-offs in terms of circuit complexity, propagation delay, and energy efficiency. The proposed ternary decoder serves as a fundamental building block for more advanced circuits such as ternary adders, multiplexers, and memory modules, making it highly suitable for modern VLSI applications where compactness, performance, and scalability are critical design goals.

**eSIM CIRCUIT**




**Figure(c):Ternary Decoder using eSim**

**OUTPUT WAVEFORM**




**Fig(d):Output waveforms of Ternary Decoder**

**Key observation of this graph:**

1. The ternary input signal clearly transitions through three distinct logic states: **0 (0 V), 1 (~0.9 V), and 2 (~1.8 V)** over the simulation period.
2. Output **A0** is active (logic HIGH) only when the ternary input is at state **0**, and remains LOW for all other input states.
3. Output **A1** becomes HIGH exclusively when the ternary input is at state **1**, showing correct one-hot decoding behavior.
4. Output **A2** is HIGH only when the ternary input reaches state **2**, validating proper ternary decoding.
5. At any given time, **only one output line (A0, A1, or A2) is HIGH**, while the others remain LOW, ensuring accurate selection.
6. The transitions between outputs occur exactly at the **input state change boundaries (10 ns and 20 ns)**, showing correct timing response.
7. The decoder successfully demonstrates **mutual exclusivity and proper functionality** for ternary inputs, confirming reliable operation of the design.

**Applications of Ternary Decoder:**

1. **Ternary Memory Addressing** – Used to select specific memory locations in multi-valued memory systems.
2. **Arithmetic Circuits** – Forms the basis for designing ternary adders, subtractors, and multipliers.
3. **Multiplexers / Demultiplexers** – Enables routing of multi-valued signals in complex digital systems.
4. **Ternary Logic Systems** – Serves as a core component in building multi-valued processors and logic circuits.

5. **Digital Signal Processing (DSP)** – Helps implement efficient data handling with fewer interconnections.
6. **VLSI Systems** – Reduces chip area and interconnect complexity in large-scale integration.
7. **Low-Power Circuits** – Provides energy-efficient decoding for portable and embedded applications.
8. **Communication Systems** – Supports multi-level signaling schemes for higher data transmission rates.

## CONCLUSION:

The design and analysis of the ternary decoder using CMOS Double Pass Logic (DPL) successfully demonstrate its capability to extend binary decoding into the domain of multi-valued logic, providing accurate, fast, and power-efficient operation. By decoding three distinct input states (0, 1, and 2) into unique one-hot outputs, the proposed architecture reduces interconnection complexity, minimizes transistor count, and enhances overall area efficiency in comparison to conventional binary decoders. Simulation results validate its correct functionality, highlighting its suitability for applications requiring compact, high-speed, and low-power multi-valued circuits.Furthermore, the comparative study with binary and other multi-valued logic approaches emphasizes the trade-offs in terms of circuit complexity, delay, and energy efficiency, offering valuable insights for the selection of architectures in future VLSI systems. The ternary decoder proves to be a versatile building block that can be effectively integrated into larger ternary systems, including adders, multiplexers, memory modules, and arithmetic units.Overall, this project establishes the proposed ternary decoder as a reliable, efficient, and scalable solution for modern VLSI design, thereby contributing to the advancement of multi-valued logic and paving the way for next-generation high-performance digital systems.

## REFERENCE:

1.https://ieeexplore.ieee.org/document/8672698