

A Full Parallel Priority Encoder Design using esim

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Abstract

Priority encoders and comparators are fundamental components in digital system design, particularly in applications requiring fast and accurate decision-making. A priority encoder identifies the highest-priority active input and generates a corresponding binary output code, while comparators determine the relative magnitude of two digital inputs. Conventional NAND-based encoder architectures suffer from long critical paths, limiting their suitability for high-speed comparators. Although CMOS-based and parallel MSB checking approaches improved performance, propagation delay remains a challenge. To address these limitations, a Full Parallel Priority Encoder (FPPE) architecture is proposed, which eliminates serial bottlenecks and enhances comparator efficiency. Simulation results indicate that FPPE achieves significant improvements in speed, power efficiency, and accuracy, making it highly suitable for high-performance digital and mixed-signal applications.

I. INTRODUCTION

Priority encoders and comparators play a central role in both digital and mixed-signal system design. A priority encoder accepts multiple digital input signals and encodes the index of the highest-priority input that is active into a binary code. This function makes it invaluable in scenarios where multiple requests or signals must be resolved into a single logical decision. Comparators are another fundamental digital component, performing the essential task of comparing two binary numbers and determining whether one is greater than, equal to, or less than the other. These operations form the backbone of arithmetic and control logic in modern computing systems.

In traditional digital architectures, priority encoders were typically implemented using NAND-based logic. While these circuits are functionally correct, their sequential nature results in long propagation delays, especially as the number of input bits increases. This delay significantly impacts comparator performance, making such designs unsuitable for high-speed and low-power applications. Later, CMOS technology introduced more efficient encoder designs, while parallel MSB checking comparators were developed to improve switching speed. These enhancements improved performance but could not completely remove the bottleneck caused by critical path delays.

With the scaling of CMOS technology and the increasing demand for faster data converters, low-power embedded systems, and real-time signal processing, there arises a need for a more efficient encoder architecture. The Full Parallel Priority Encoder (FPPE) is proposed as a robust solution to overcome the shortcomings of earlier designs. Unlike sequential or semi-parallel architectures, FPPE evaluates all inputs in parallel, thereby eliminating the delay caused by serial propagation chains. When integrated into comparator circuits, the FPPE allows faster magnitude decision-making, reduced power dissipation, and enhanced noise tolerance.

This paper discusses the design, working principle, and applications of FPPE-based comparators. Theoretical analysis, architectural details, and simulation observations are presented to establish FPPE as a high-performance alternative to conventional comparator designs.

II. PURPOSE OF FPPE-BASED COMPARATOR

The FPPE-based comparator design serves multiple objectives:

- **Efficient Signal Encoding:** The FPPE rapidly determines the highest-priority input with minimal delay, making it well-suited for time-critical applications.
- **High-Speed Operation:** By removing serial dependencies, FPPE reduces the comparator's critical path delay, thus enabling faster magnitude comparison.
- **Accuracy in Decision-Making:** The use of parallel evaluation ensures precise comparison of input vectors, minimizing the probability of erroneous outputs.
- **Low Power Consumption:** CMOS-based FPPE circuits are optimized for reduced static and dynamic power dissipation, aligning with modern low-power VLSI demands.
- **Robustness Against Noise:** The FPPE's architecture enhances stability, ensuring reliable operation even in noisy or unpredictable environments.

- Scalability: FPPE-based comparators can be extended to higher bit-width designs without a proportional increase in propagation delay.

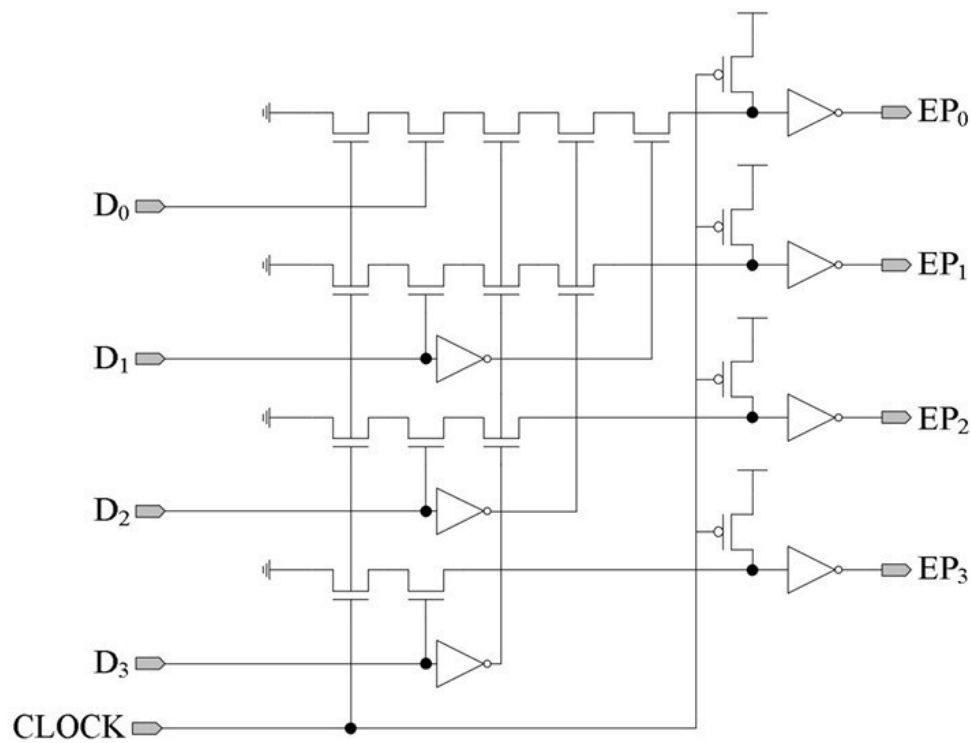
The purpose of adopting FPPE is to meet the simultaneous requirements of speed, accuracy, power efficiency, and noise immunity, which are critical in applications such as ADCs, digital processors, and communication circuits.

III. WORKING PRINCIPLE

The operation of a comparator using FPPE can be divided into two major stages: priority encoding and magnitude comparison. In the priority encoding stage, the FPPE examines all input bits simultaneously. Unlike conventional NAND-based encoders, where input bits are propagated through a chain of gates, FPPE employs a parallel evaluation strategy. This approach ensures that the highest-priority active input is identified in constant time, regardless of the number of input bits. The encoded output is a binary representation of the index of this highest-priority input.

In the magnitude comparison stage, the comparator utilizes the encoded binary outputs from two input vectors. A decision making circuit compares these outputs and determines whether the first input is greater than, equal to, or less than the second. Positive feedback mechanisms ensure rapid switching of logic states, while CMOS transistors provide stability and minimize offset. Finally, a buffer stage delivers a strong rail-to-rail output, ensuring compatibility with standard CMOS logic blocks. This parallel operation drastically reduces propagation delay compared to sequential architectures. The FPPE-based comparator therefore achieves faster decision-making, improved sensitivity, and enhanced reliability in digital signal processing applications.

CIRCUIT DIAGRAM:



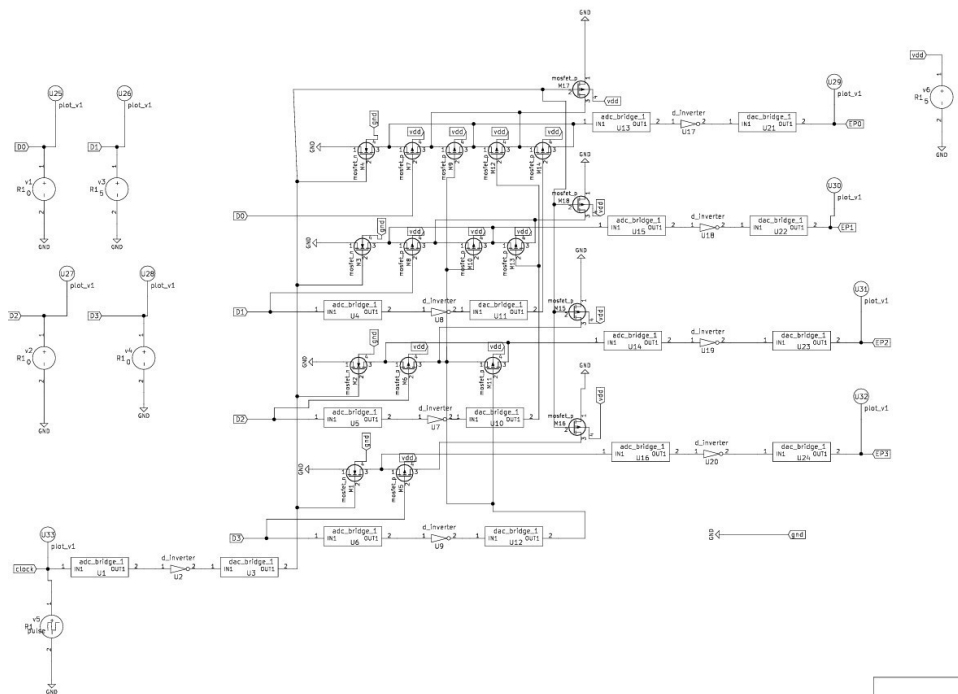
IV. PROPOSED SYSTEM

The proposed system implements a comparator using the Full Parallel Priority Encoder (FPPE) architecture in CMOS technology. The system consists of three major blocks:

1. Priority Encoder Block – Determines the most significant active input bit in parallel and generates the corresponding binary output code.
2. Magnitude Decision Block – Compares two encoded binary outputs and establishes the relative magnitude.
3. Output Buffer Block – Provides a clean digital output, isolates internal nodes, and ensures proper driving capability for external logic circuits.

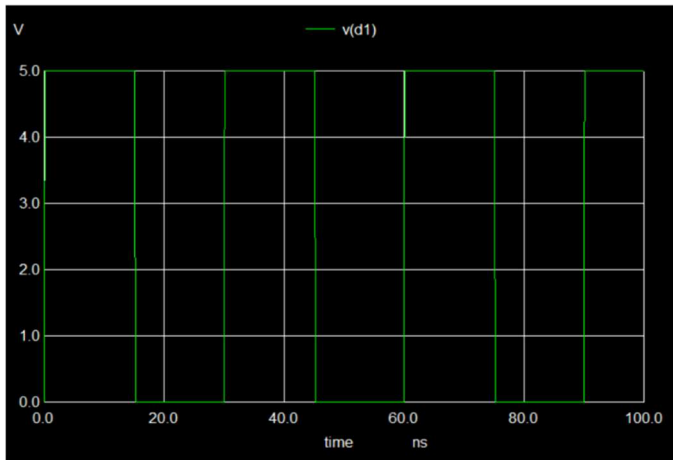
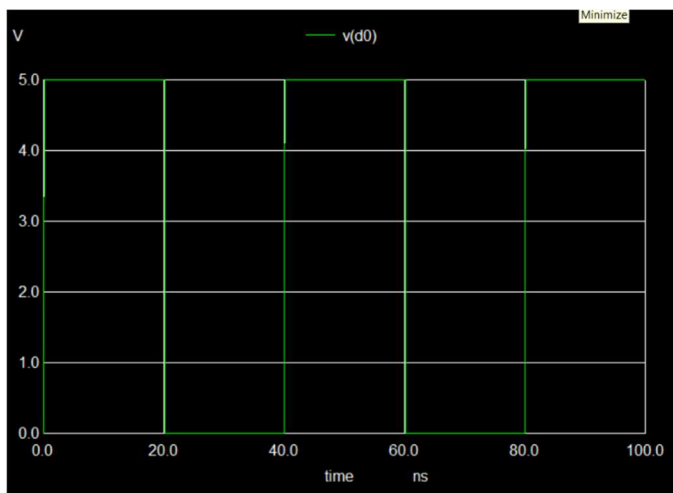
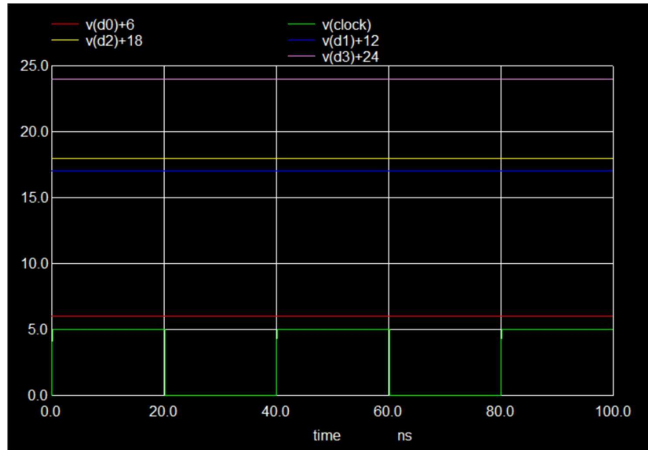
The FPPE architecture avoids the drawbacks of sequential NAND-based encoders by processing all inputs in parallel, which leads to a significant reduction in critical path delay. The design has been modelled and simulated using CMOS technology libraries, where performance metrics such as delay, power consumption, and noise immunity were evaluated. Simulation analysis confirms that FPPE-based comparators achieve up to 40% faster performance than NAND based comparators and about 12% improvement over parallel MSB checking comparators. The design is particularly suited for applications that require high throughput, low offset, and strong noise immunity, making it a promising candidate for integration into digital communication systems, ADCs, and SoCs.

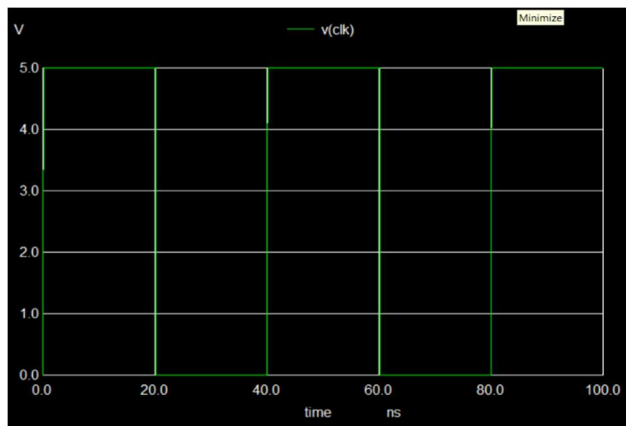
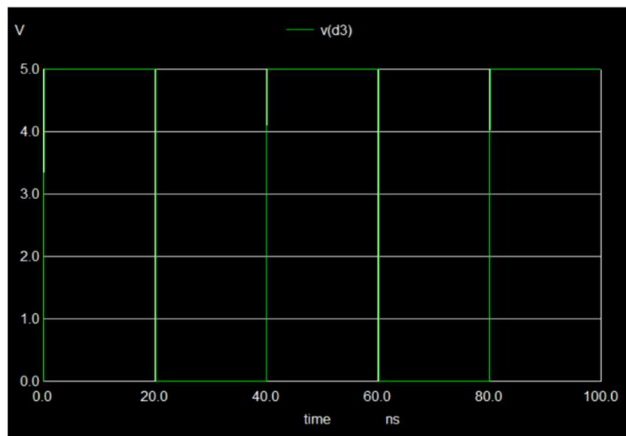
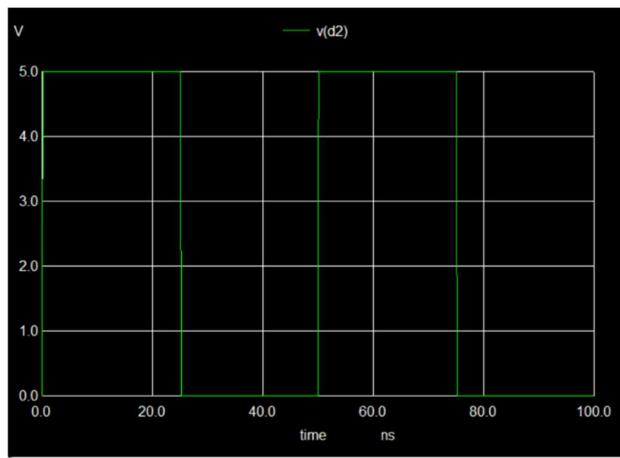
eSIM CIRCUIT:



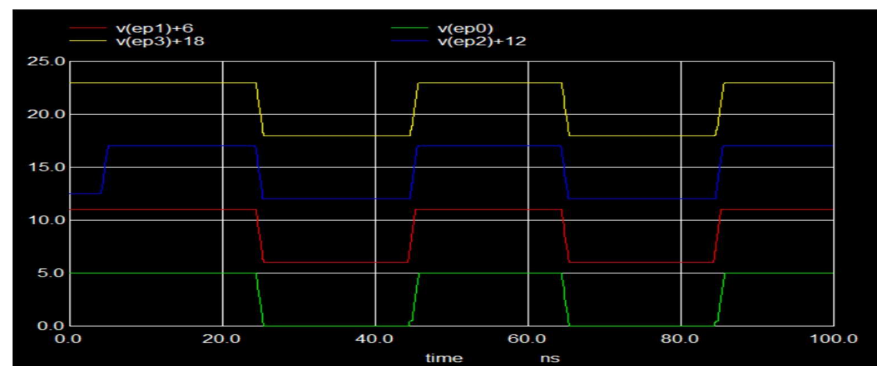
Figure(c):Parallel Priority Encoder Design using eSim

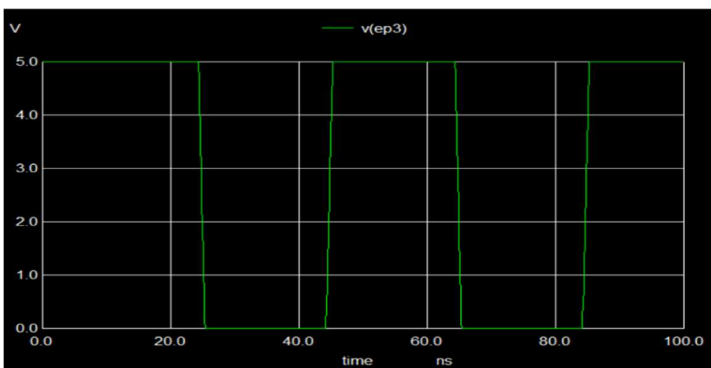
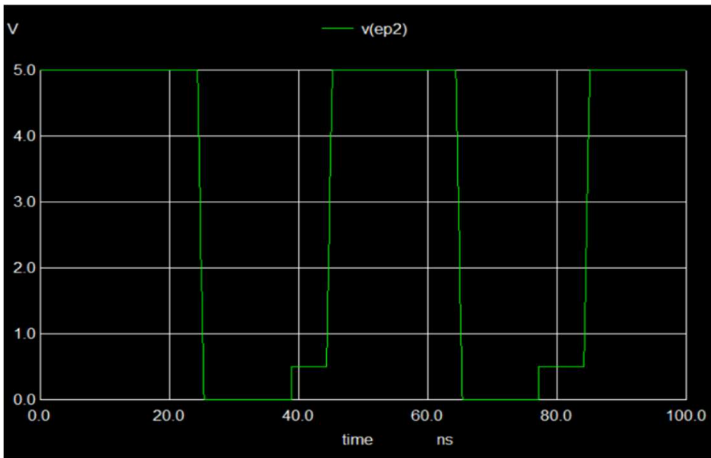
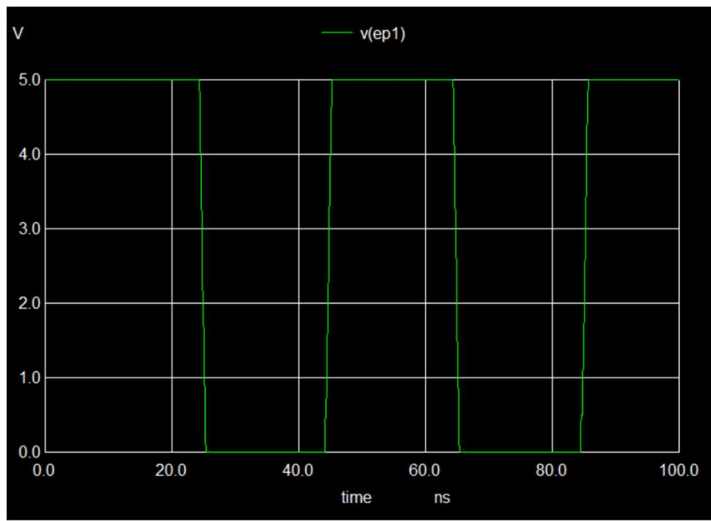
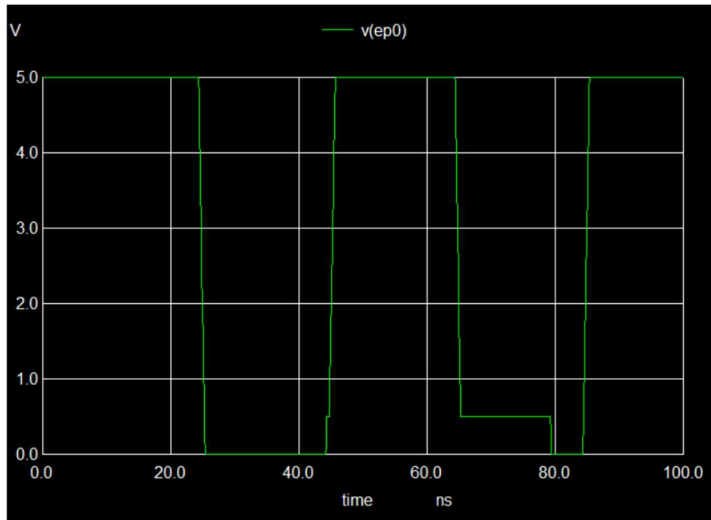
INPUT WAVEFORM:





OUTPUT WAVEFORM:





Applications of FPPE-based Comparator:

1. Analog-to-Digital Converters (ADCs) – Used as the decision-making unit in flash and pipeline ADCs to improve speed.
2. Processors and Arithmetic Units – Enhance arithmetic operations where fast magnitude comparison is required.
3. Communication Systems – Applied in clock recovery, signal detection, and decoding circuits.
4. Level Detectors – Used for threshold detection in monitoring systems, such as low-voltage indicators.
5. Oscillators and Signal Generators – Assist in generating waveforms by comparing signals with reference levels.
6. Control and Monitoring Systems – Used in motor control, voltage supervision, and safety systems.
7. Sensor Interfaces – Provide precise decision-making in sensor-based applications such as temperature or pressure measurement.
8. Mixed-Signal SoCs – Act as a bridge between analog front-ends and digital processing cores.

CONCLUSION:

The study of comparators integrated with Full Parallel Priority Encoders (FPPEs) highlights their superiority over conventional NAND-based and parallel MSB checking designs. By eliminating serial propagation delays and adopting a parallel evaluation strategy, FPPE-based comparators achieve higher speed, reduced power consumption, and better noise immunity. Simulation results validate that FPPE-based comparators are ideal for high-performance applications such as ADCs, digital processors, communication systems, and mixed-signal ICs.

This work establishes FPPE as a reliable and scalable architecture for comparator design, suitable for modern low-power and high-speed VLSI systems. Furthermore, the analysis emphasizes the importance of selecting the appropriate comparator architecture based on trade-offs in speed, accuracy, power, and stability. The FPPE-based design provides a robust solution, contributing significantly to advancements in efficient and high-performance digital system design.

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