

Transient analysis of three-stage comparator using eSim

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Abstract

Comparators are fundamental building blocks in analog and mixed-signal circuits, as they perform the essential function of comparing two analog input signals and producing a binary output. Owing to this property, they are often regarded as one-bit analog-to-digital converters (ADCs). Comparators are widely employed in a variety of applications including data conversion systems, level shifters, relaxation oscillators, window detectors, and null detectors. The increasing demand for high-speed, low-power, and high-precision circuits has made the design of efficient comparators a critical area of research.

This paper presents the design and performance analysis of a three-stage conventional comparator, which consists of a preamplifier stage, a decision-making stage, and an output buffer stage. The preamplifier stage reduces input-referred offset and enhances sensitivity, the decision stage ensures fast switching between logic levels, and the buffer stage provides sufficient drive capability for subsequent digital circuits. The proposed comparator has been implemented using 90-nm CMOS technology with eSim software.

In addition to the design of the conventional comparator, the paper discusses its comparison with two other popular architectures: the latch-based comparator and the hysteresis-based comparator. Each architecture is evaluated in terms of key performance parameters such as propagation delay, power consumption, offset voltage, and noise immunity. While latch-based comparators offer high-speed operation and reduced power dissipation, hysteresis-based comparators improve stability in noisy environments. The results highlight the trade-offs involved in selecting the appropriate comparator design for different applications.

Through simulation and analysis, this work aims to provide a clear understanding of the design considerations, advantages, and limitations of various comparator architectures in modern CMOS technology. The proposed study serves as a useful reference for engineers and researchers working on high-performance ADCs and related mixed-signal systems.

I. INTRODUCTION

Comparators are essential building blocks in analog and mixed-signal circuits, widely used for converting continuous-time analog signals into discrete-time digital logic outputs. Functionally, a comparator operates as a one-bit analog-to-digital converter (ADC) by comparing two input voltages and producing a binary output depending on their relative magnitudes. This fundamental property makes comparators indispensable in a wide range of applications including high-speed ADCs, level shifters, relaxation oscillators, window detectors, and signal processing systems. With the continuous scaling of CMOS technology, the design of comparators has gained significant attention due to the simultaneous need for **low power consumption, high speed, precision, and reduced offset voltage**. Traditional comparator architectures include **open-loop comparators**, which offer simplicity but suffer from limited speed, and **regenerative comparators**, which achieve faster operation but may face challenges in terms of offset and noise sensitivity. Hybrid architectures have also been developed to combine the advantages of both. This review focuses on the design and analysis of a **three-stage conventional comparator**, which consists of a **preamplifier stage, a decision-making latch stage, and an output buffer stage**. The preamplifier reduces offset and enhances sensitivity, the latch provides rapid decision-making through positive feedback, and the buffer ensures reliable digital output with sufficient driving capability. The comparator has been designed in **90-nm CMOS technology** using **eSim software**. In addition to the conventional design, the study compares its performance with **latch-based** and **hysteresis-based** comparators to highlight trade-offs in terms of **speed, offset, noise immunity, and power efficiency**. Such comparisons are crucial for selecting the appropriate architecture for specific applications in modern high-performance ADCs and mixed-signal systems.

II. PURPOSE OF THREE STAGE COMPARATOR

The purpose of this three-stage comparator circuit is:

- **Signal Comparison** – It compares two analog input signals (inverting and non-inverting) and determines which one is greater.
- **Analog-to-Digital Conversion (1-bit)** – Acts as a one-bit ADC, producing a digital output (logic high or low) depending on the input difference.
- **High Sensitivity and Accuracy** – The **preamplifier stage** reduces input offset and enhances small signal differences, ensuring accurate decision-making.
- **Fast Decision Making** – The **regenerative latch stage** provides positive feedback, rapidly amplifying the input difference to a full-swing digital output.
- **Strong Output Drive** – The **buffer stage** isolates internal nodes and ensures the comparator can reliably drive external CMOS logic circuits or digital blocks.

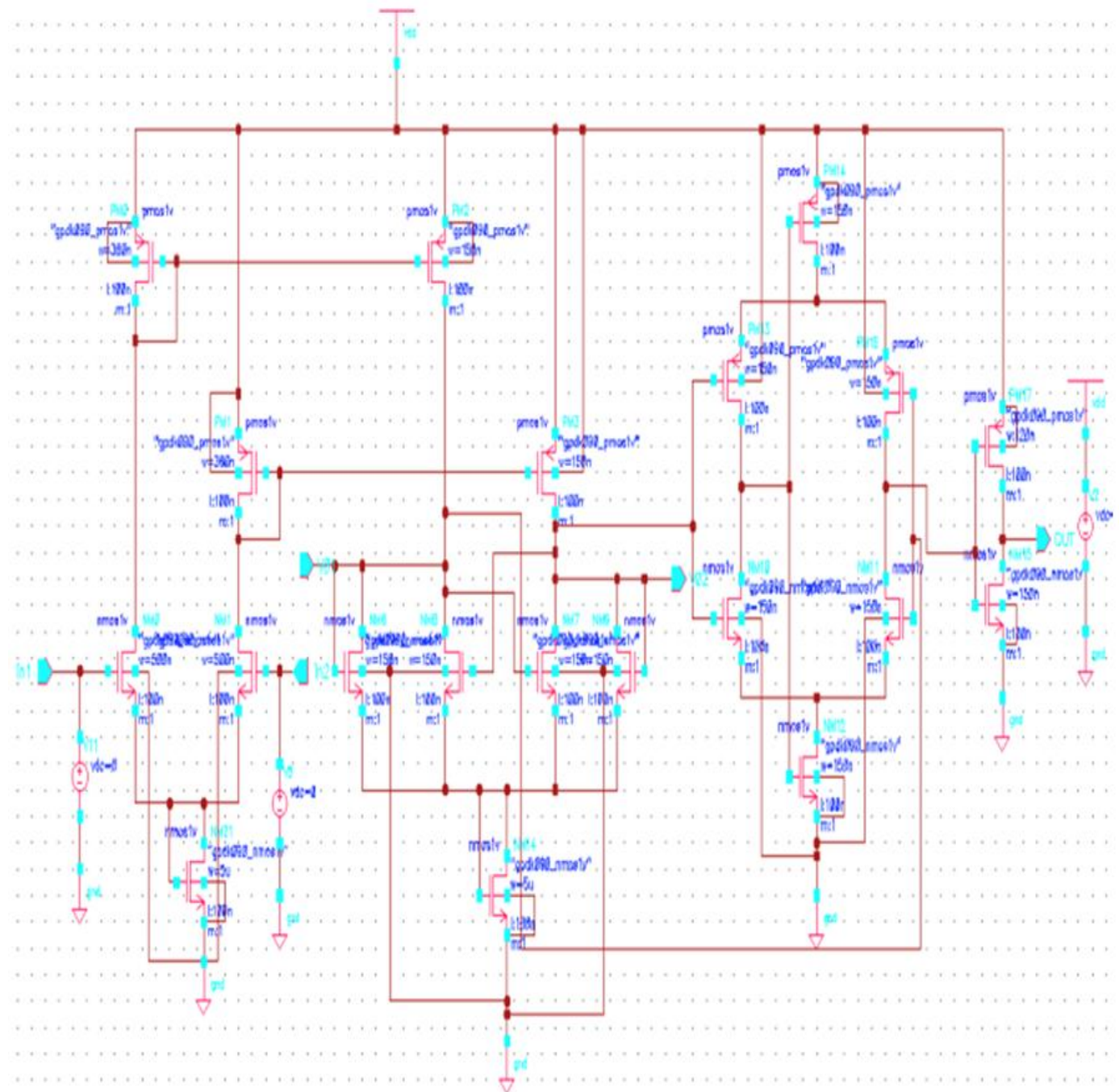
III. WORKING PRINCIPLE

The working principle of a Cockcroft–Walton voltage multiplier is based on the sequential charging and discharging of capacitors through diodes to progressively increase the DC output voltage from an AC input source. Here are the key steps in its operation:

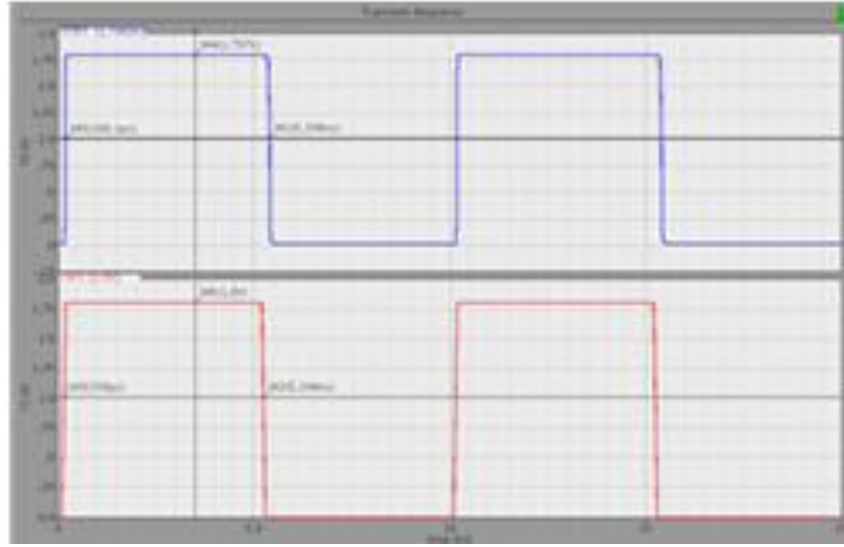
1. **Input AC Voltage Application:** When an alternating voltage is applied to the circuit, the diodes and capacitors are arranged in such a way that during each half-cycle, specific capacitors are charged to the peak AC voltage.

2. **Charging During Positive Half-Cycle:** In the positive half of the AC input, certain diodes become forward-biased, allowing current to flow and charge the corresponding capacitors to the peak voltage value.
3. **Charging During Negative Half-Cycle:** In the negative half of the AC input, a different set of diodes conducts, transferring the charge from previously charged capacitors to the next stage, effectively stacking the voltages.
4. **Voltage Multiplication:** As the process repeats over multiple AC cycles, each stage adds to the total output voltage. The output voltage is approximately equal to twice the peak input voltage multiplied by the number of stages, minus small drops due to diode forward voltage and load effects.
5. **Stable High-Voltage Output:** Under light-load conditions, the output voltage remains nearly constant with minimal ripple. However, heavy loads can cause voltage sag due to capacitor discharge between cycles, which can be minimized by using larger capacitors or higher operating frequencies.
6. **Practical Applications:** This principle makes the circuit ideal for generating high DC voltages in applications such as particle accelerators, X-ray generators, electrostatic equipment, and high-voltage testing devices.

CIRCUIT DIAGRAM



Figure(a)



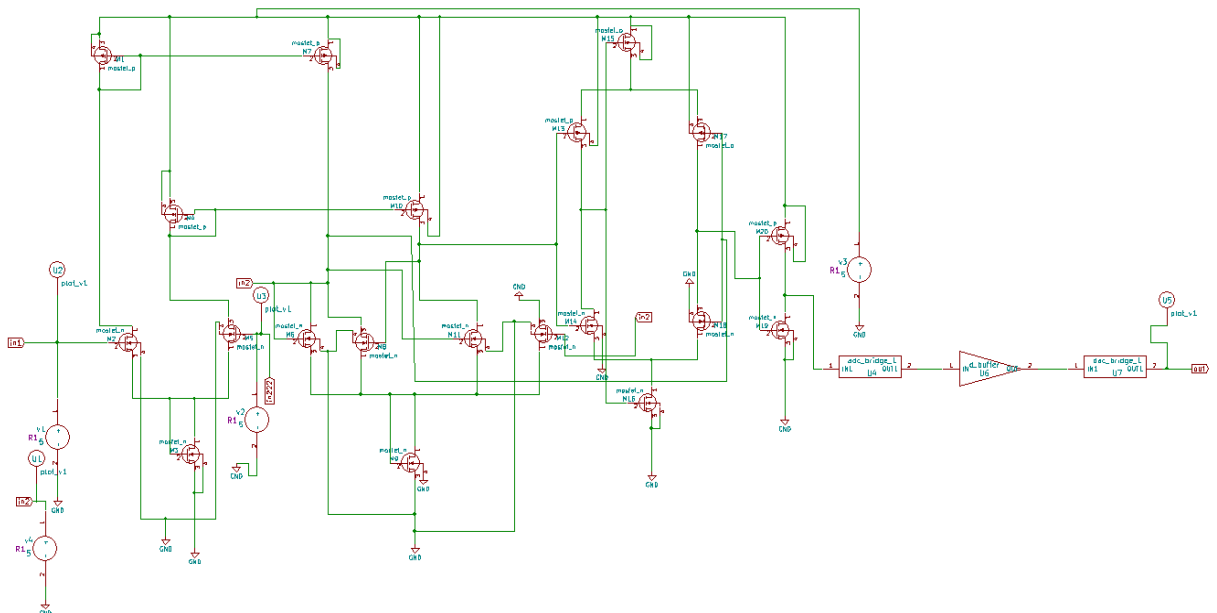
Figure(b)

Fig.a: Circuit of Three stage Comparator

IV. PROPOSED SYSTEM

The proposed system focuses on the design and implementation of a **three-stage conventional comparator** using **90-nm CMOS technology** with the **Cadence Virtuoso (gpd90 library)** platform. The architecture is composed of three essential stages: a **preamplifier**, a **decision-making latch**, and an **output buffer**. The preamplifier stage plays a crucial role in enhancing small input voltage differences while minimizing input-referred offset, thereby improving the overall accuracy of the comparator. The decision-making stage, implemented as a regenerative latch, employs positive feedback to rapidly convert the amplified analog difference into a clear digital logic state, ensuring high-speed operation. Finally, the output buffer stage provides the necessary drive strength and isolates the comparator's internal nodes, producing a clean rail-to-rail digital output compatible with standard CMOS logic. This structured approach ensures that the comparator achieves **low offset, fast response, and high noise immunity**, which are vital for precision applications. In addition, the design has been evaluated against **latch-based** and **hysteresis-based comparators** to highlight trade-offs in terms of speed, stability, and power consumption. The proposed comparator is well-suited for integration into **analog-to-digital converters (ADCs)**, **signal conditioning circuits**, **oscillators**, and **threshold detection systems**, making it a robust and versatile solution for modern mixed-signal electronic applications.

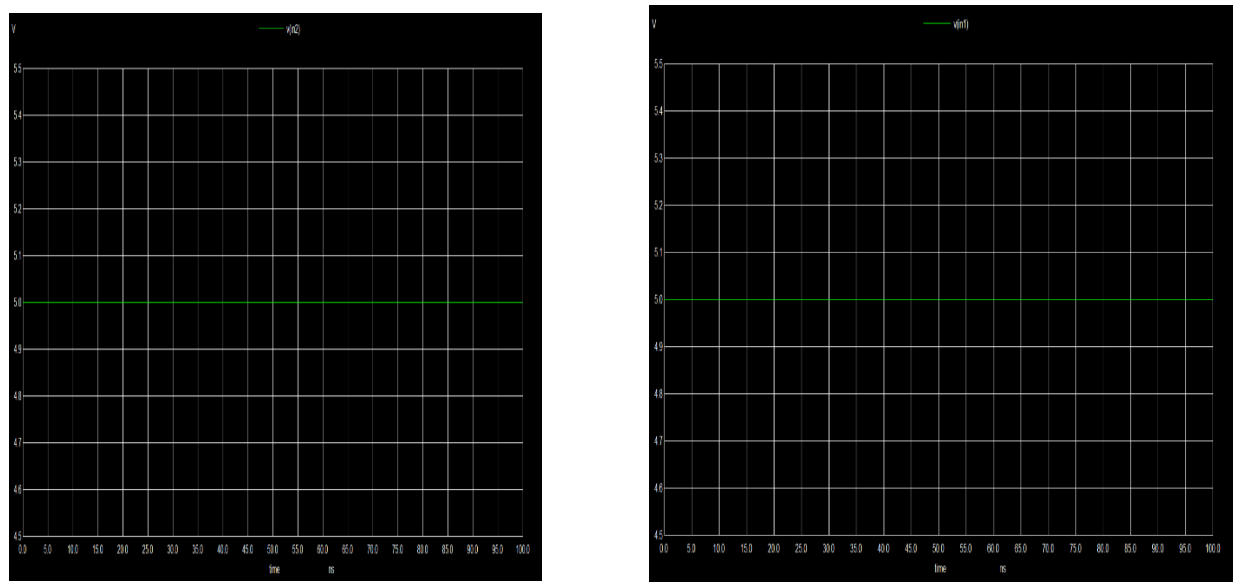
eSIM CIRCUIT



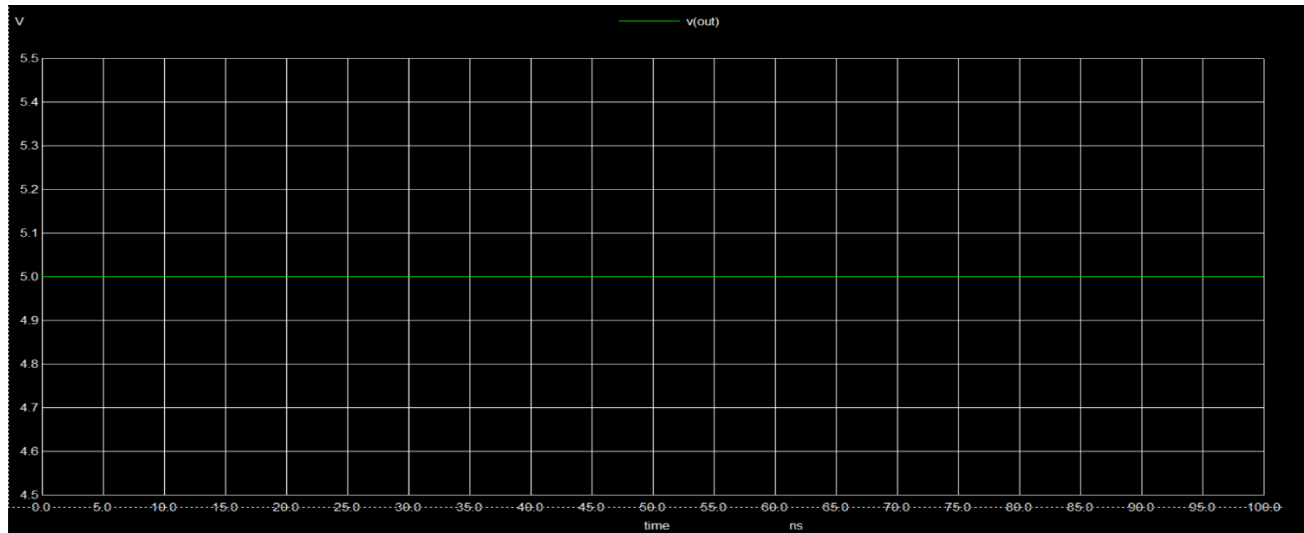
Figure(c):Three stage comparator using eSim

Figure 2 presents the circuit diagram of a **CMOS-based logic circuit** designed and simulated using **eSim**, an open-source EDA tool. The schematic consists of PMOS and NMOS transistors arranged to form pull-up and pull-down networks, which implement a digital logic function at the transistor level. The inputs are applied through voltage sources and passed into the transistor network, where the MOSFETs act as switches to realize the required logic operation. To enable **mixed-signal simulation**, the design includes **ADC and DAC bridges** along with a buffer stage, which help in converting signals between analog and digital domains for proper co-simulation in eSim. The output is finally observed at the plotting terminal, allowing verification of the circuit behavior. This design demonstrates how **transistor-level CMOS logic** can be implemented, tested, and analyzed in both analog and digital domains using eSim.

INPUT WAVEFORM:



OUTPUT WAVEFORM:



Fig(d):Output waveforms of Transient analysis of three-stage comparator

Figure 3 showcases the output waveform of the circuit is plotted as a constant line at approximately **5 V**, which corresponds to a logic high state in digital design. Throughout the entire simulation window, the voltage does not exhibit any transitions or variations, indicating that the output node is continuously maintained at a high logic level. This behavior highlights that under the given input and biasing conditions, the pull-up network of the CMOS circuit dominates, ensuring that the output remains connected to the supply rail. The absence of any switching activity also suggests that the inputs applied during simulation did not reach values necessary to activate the pull-down path, thereby preventing the output from going low. Such a flat waveform can arise due to several factors, including constant logic inputs, improper signal excitation, or the nature of the designed logic circuit which may inherently produce a fixed high output for certain combinations of inputs. In practical terms, this result confirms that the circuit responds deterministically to the chosen test conditions. However, to fully analyze its switching behavior, it would be necessary to apply varying input pulses so that changes in output logic levels, if any, can be observed and validated against the expected logic function.

Key observation of this graph:

1. The output voltage remains constant at 5 V throughout the entire simulation period.
2. The waveform is a flat line, showing no switching activity or variation over time.
3. The circuit output corresponds to a logic HIGH state for the applied input conditions.
4. No logic transitions (0 to 1 or 1 to 0) are observed within the simulation window.
5. This behavior indicates that the pull-up network dominates, keeping the output tied to VDD.
6. The absence of transitions may be due to constant inputs, lack of input excitation, or the circuit being designed to hold a fixed HIGH state.

Applications of three stage comparator:

1. Analog-to-Digital Converters (ADCs) – Used in flash, pipeline, and successive approximation ADCs as the decision-making element.
2. Level Detectors / Threshold Detectors – Detects whether an input signal exceeds a reference level (e.g., battery low indicator).
3. Window Detectors – Compares signals against two reference voltages to check if they lie within a specified range.
4. Oscillators – Used in relaxation oscillators and waveform generators.
5. Zero-Crossing Detectors / Null Detectors – Detects when an input signal crosses zero, widely used in control systems.
6. Signal Conditioning Circuits – Converts small analog differences into clean digital signals.
7. Communication Systems – Used in data recovery, clock extraction, and signal slicing.
8. Control and Monitoring Systems – Applied in motor controllers, voltage monitoring, and protection circuits.
9. Sensor Interfaces – Processes signals from sensors (temperature, pressure, etc.) by comparing them with reference levels.
10. Mixed-Signal ICs – Acts as an interface between analog and digital subsystems in SoCs.

CONCLUSION:

The design and analysis of the three-stage conventional comparator in 90-nm CMOS technology successfully demonstrate its effectiveness in achieving accurate, fast, and reliable analog signal comparison. By integrating a preamplifier stage, a decision-making latch stage, and an output buffer stage, the proposed architecture reduces input offset, enhances sensitivity, ensures rapid decision-making, and delivers a clean digital output with strong driving capability. Simulation results validate its suitability for applications demanding low offset, high speed, and improved noise immunity. Furthermore, the comparative study with latch-based and hysteresis-based comparators highlights the trade-offs in terms of speed, stability, and power efficiency, offering insights into appropriate architecture selection for specific applications. The three-stage comparator proves to be highly versatile and can be effectively used in ADCs, signal conditioning circuits, window detectors, oscillators, and control systems. Overall, this project establishes the proposed comparator design as a robust, efficient, and application-ready solution for modern mixed-signal and digital systems, thereby contributing to advancements in low-power, high-performance VLSI design.

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