# Design and Simulation of a Low-Voltage Cross-Coupled Charge Pump

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## Abstract

This paper explores the design, modeling, and simulation of a two-phase cross-coupled CMOS AC-DC charge pump operating in the subthreshold region. The architecture is widely favored for low-voltage energy-harvesting applications due to its improved pumping efficiency and lower threshold voltage drop compared to conventional diode-based charge pumps. Using complementary clock signals to drive cascaded stages of cross-coupled MOSFET pairs, charge is transferred progressively, resulting in a boosted DC output voltage. The analysis includes circuit topology, device modeling, and transient response simulation, demonstrating the feasibility of achieving high output resistance and stable DC voltage applicable to IoT and biomedical systems.

**Keywords: Cross-coupled charge pump, AC-DC conversion, energy harvesting, CMOS, subthreshold operation.**

## I. INTRODUCTION

Low supply voltages in portable and IoT devices pose challenges for efficiently generating higher operating voltages on-chip without external inductors. Traditional diode-connected charge pumps suffer from significant voltage losses and inefficiency, particularly at subthreshold operation. The problem is to design a cross-coupled charge pump with increased output resistance, enhanced voltage boosting, and reduced ripple under realistic CMOS technology constraints. This requires careful consideration of device characteristics, clocking schemes, and multi-stage charge transfer dynamics.

## II. PURPOSE OF CROSS-COUPLED CHARGE PUMP

The primary purpose of the cross-coupled charge pump is to efficiently boost low input voltages to higher DC levels without using bulky inductors. It utilizes complementary MOSFET switching pairs driven by non-overlapping clocks to transfer charge through capacitive stages. This architecture reduces voltage losses commonly seen in diode-based charge pumps by eliminating threshold voltage drops. Higher output resistance compared to traditional designs improves voltage stability and power efficiency. The cross-coupled design is particularly suited for low-power and energy harvesting applications, such as IoT devices and biomedical implants. By leveraging subthreshold CMOS device operation, it achieves effective charge transfer with minimal power consumption. Ultimately, it provides a compact, integrable solution for on-chip voltage multiplication in modern electronic systems.

## III. WORKING PRINCIPLE

The Cross-Coupled Charge Pump operates by transferring charge through complementary pairs of MOSFET switches and capacitors driven by two non-overlapping clock signals. These clocks alternately drive the gates of NMOS and PMOS transistors in cascaded stages.

- When first clock goes high, one set of transistors turns on,allowing the first stage capacitor to charge.
- When the clock switches low, the stored charge is transferred forward to the next stage through the activated complementary MOSFETs.
- Simultaneously, the second clock drives the next transistor pair, charging the next capacitor and continuing the charge pumping process.
- This alternating sequence continues through all stages, progressively increasing the voltage at each stage.
- The output voltage rises stage-by-stage as the capacitive charge is transferred in a latch-like fashion via cross-coupled transistor pairs.
- The cross-coupled topology effectively reduces threshold voltage drop losses compared to single diode-based pumps.
- Ultimately, the output voltage is boosted well beyond the input AC voltage, producing a stable and efficient DC output.

## IV. CIRCUIT DIAGRAM

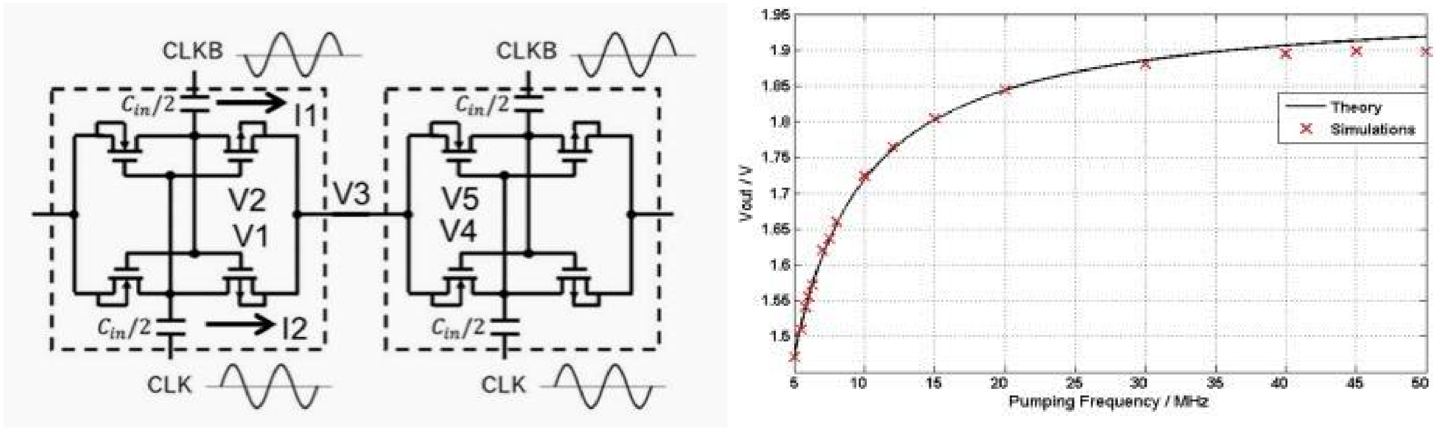


Fig. 1: Dickson charge pump with sample output waveform

This is a block diagram of a cross-coupled charge pump consisting of two cascaded stages, each driven by complementary clock signals. The arrangement of NMOS and PMOS transistors enables efficient charge transfer with alternating charge/discharge cycles. Input capacitors are split for optimized charge sharing, while CLK and CLKB waveforms ensure non-overlapping switching. As charge moves from left to right through each stage, the output DC voltage is progressively boosted beyond the input.

## V. Proposed System

The proposed system features a cross-coupled charge pump architecture using complementary MOSFET pairs driven by non-overlapping clock signals. Cascaded stages transfer charge progressively, boosting the input AC voltage to a higher DC level. Capacitors at each stage store and transfer charge with improved efficiency by reducing threshold losses seen in diode-based pumps. The system is designed for low-voltage, low-power applications such as energy harvesting and integrated IoT devices.

**eSIM CIRCUIT**

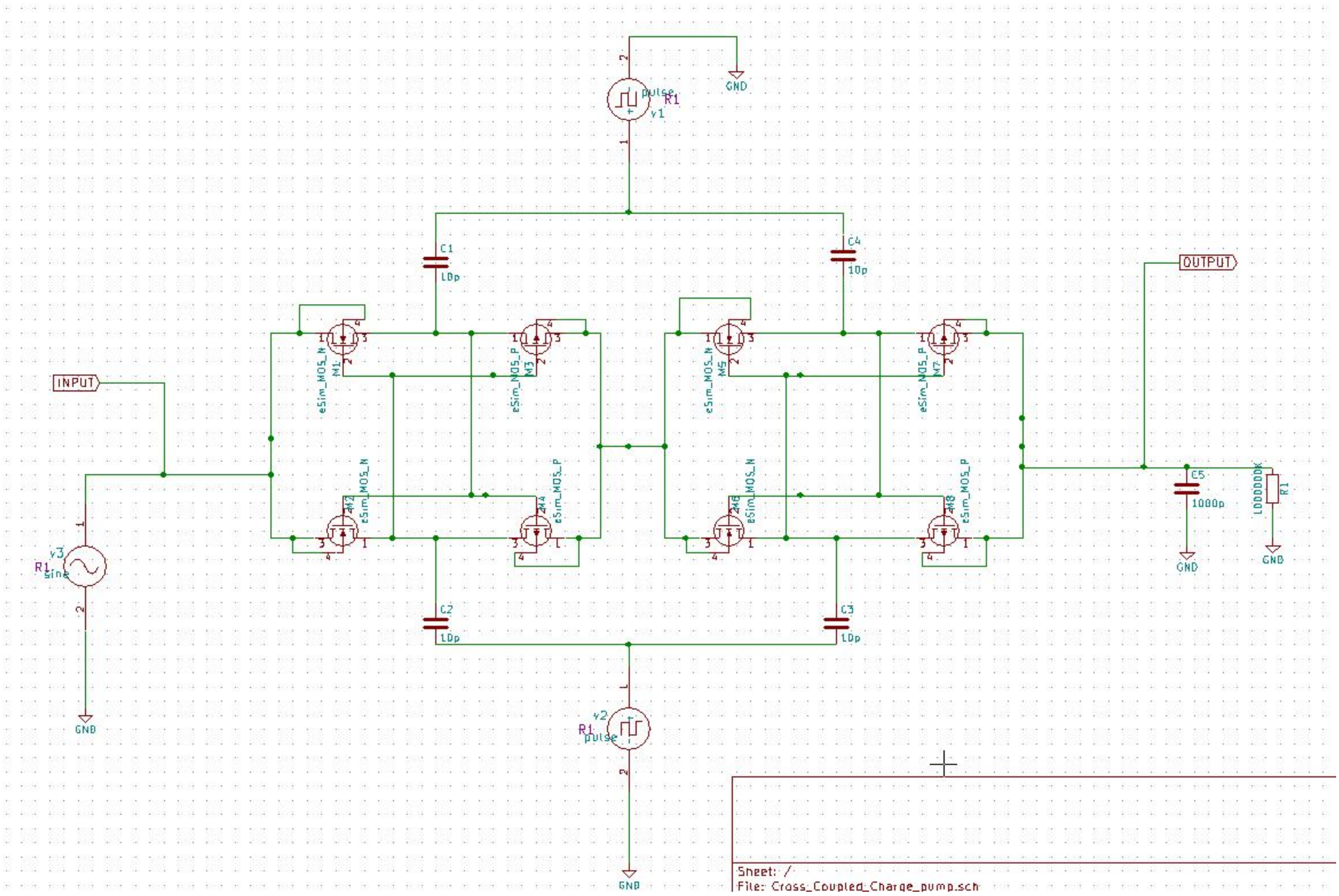


Fig. 4: Cross-Coupled Charge Pump Circuit in eSim

This is a schematic of a cross-coupled charge pump, which uses pairs of NMOS and PMOS transistors arranged in cascaded stages. Clock signals drive the gates, enabling capacitors to transfer charge sequentially from the input toward the output. An output filter capacitor and high-value load resistor smooth the boosted DC voltage produced. The design enables efficient voltage multiplication without inductors, suitable for low-power integrated circuits.

## OUTPUT WAVEFORM

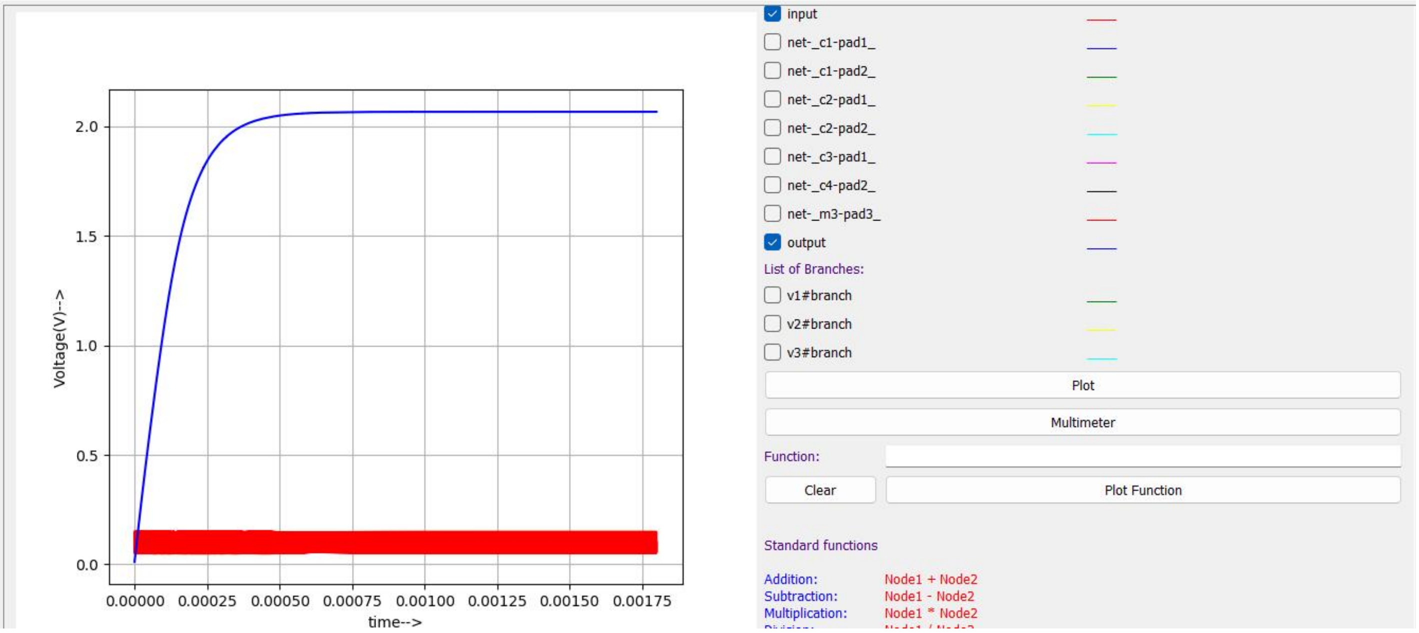


Fig. 5: Output Cross-Coupled Charge Pump Circuit in eSim

**Fig. 5** This graph displays the typical output response of a charge pump circuit over time. The voltage on the left (input) starts near zero and quickly rises, stabilizing at a higher value as the circuit reaches steady state. The input signal remains low and constant, while the output signal settles to a boosted DC level. This waveform illustrates successful voltage multiplication and filtering behavior expected from a cross-coupled charge pump.

## VI.CONCLUSION

The cross-coupled charge pump topology offers improved voltage boosting efficiency by minimizing threshold voltage losses compared to traditional diode-based designs. Its complementary MOSFET switching reduces reverse leakage currents, enhancing overall power conversion efficiency. The architecture provides higher output resistance and stable DC output with low ripple, making it suitable for low-power and energy harvesting applications. Design flexibility allows optimization for various supply voltages and load conditions. This makes it a compact, integrable choice for modern VLSI and IoT systems requiring efficient DC-DC conversion.

## VII. REFERENCE


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