Conventional 4-Bit BCD Adder

Jovin P John
Electronics and Communication Engineering
Albertian Institute of Science and Technology
Kochi, Kerala

***Abstract*— This project implements a 4-bit Binary Coded Decimal (BCD) adder for adding two single decimal digits (0-9). The design uses two cascaded 4-bit binary adders with correction logic. When the sum exceeds 9, the circuit automatically adds 6 to maintain valid BCD output format.**

Keywords*— *BCD Adder, Binary Coded Decimal, Correction Logic, Detection Circuit

I. Introduction

A 4-bit BCD Adder is a digital circuit designed to add two single decimal digits represented in BCD format. Unlike regular binary addition, BCD addition requires correction when the result exceeds 9 to maintain proper decimal representation in digital systems.

II. Objectives

The aim of this project is to design a 4-bit BCD adder that correctly adds two BCD numbers with carry input. The project focuses on implementing correction logic that detects when the sum exceeds valid BCD range and automatically applies the necessary correction. The goal is to build the truth table, run transient analysis simulation, and confirm that the adder works as expected.

III. Implementation

The BCD adder uses two cascaded 4-bit binary adders. The first performs normal binary addition, while detection logic (C4 + S3·S2 + S3·S1) determines if correction is needed. When triggered, the second adder adds 6 to convert the result back to valid BCD format.

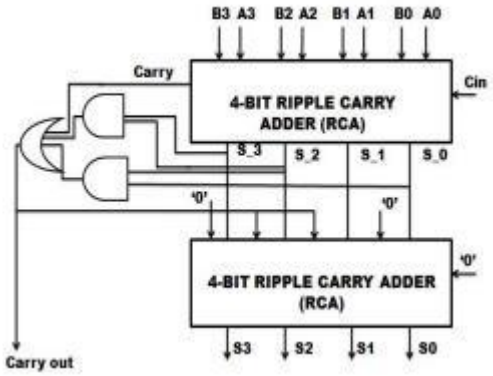

Fig. 2. Logic Diagram

IV. Results

The 4-bit BCD Adder was implemented and tested in eSim. The truth table was prepared with inputs ranging from 1001 down to 0000, and the outputs of sum, carry, and detection logic were verified through transient analysis. The results confirm that the adder performs correct BCD addition for all cases. Transient analysis showed that the detection logic properly identifies when correction is required.

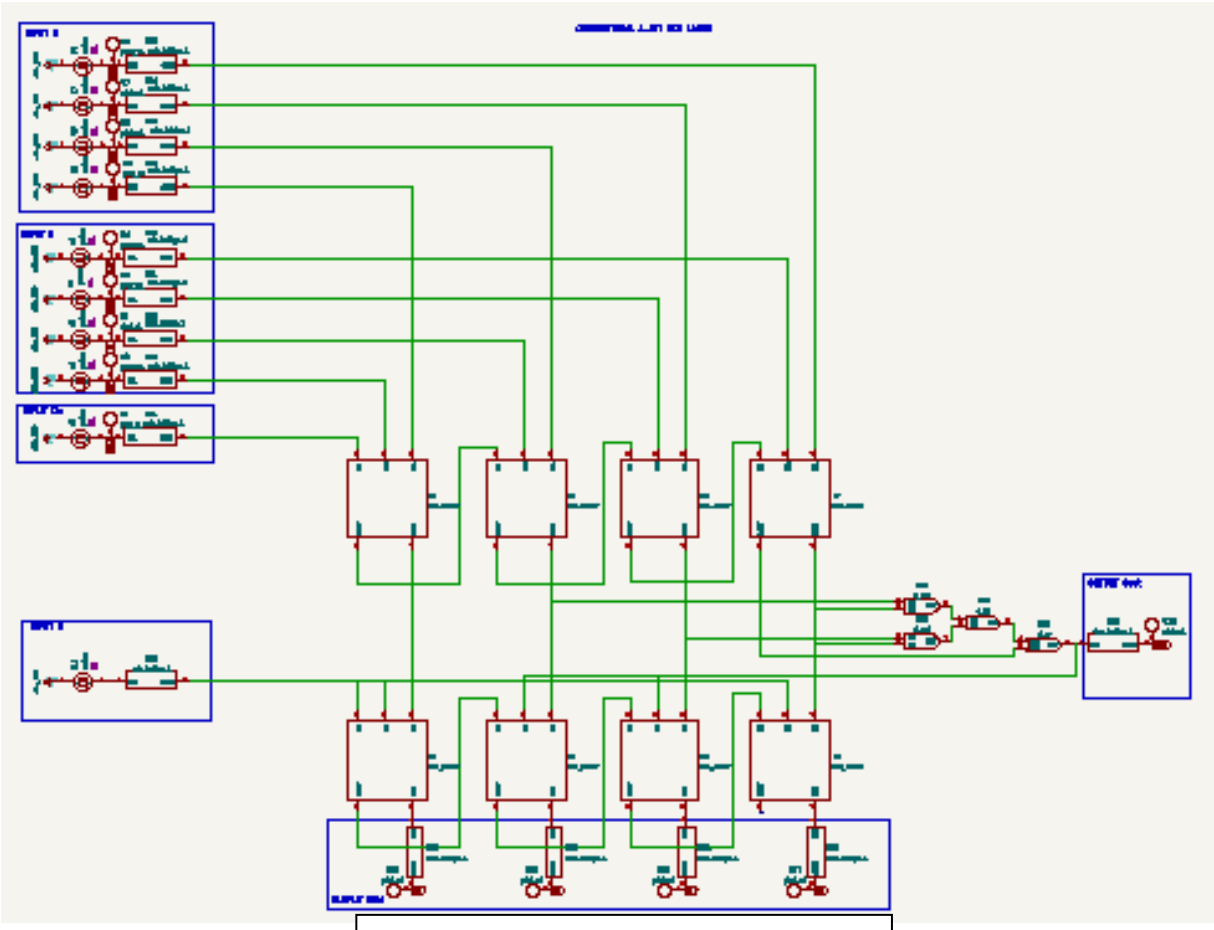

Fig. 1. eSim Circuit Schematic

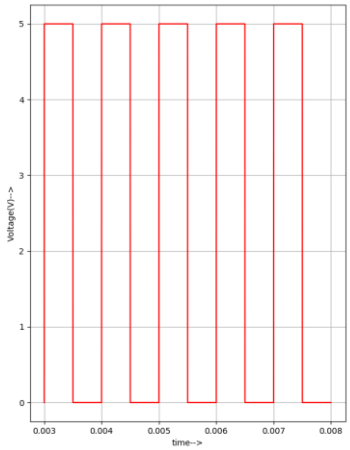

Fig. 3. Input A0

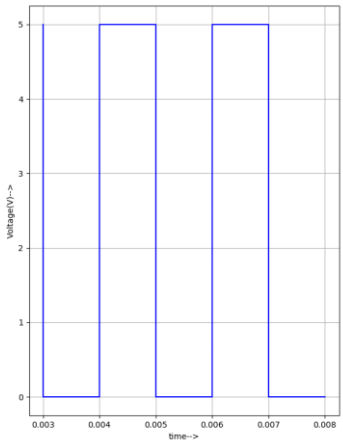

Fig. 4. Input A1

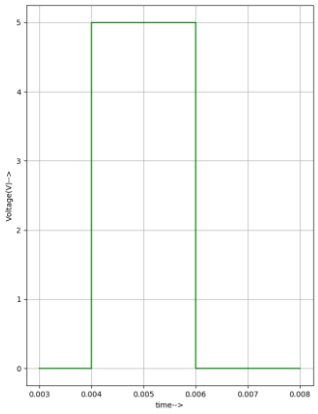

Fig. 5. Input A2

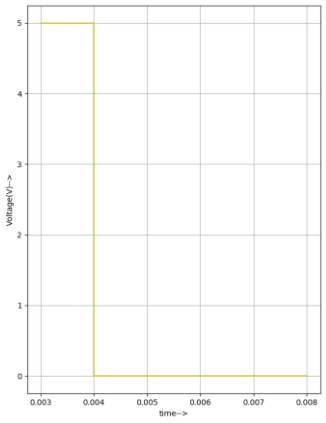

Fig. 6. Input A4

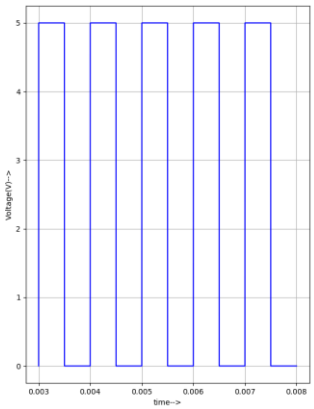

Fig. 7. Input Carry

Figures 3, 4, 5, 6 and 7 represent the four input bits of A, and carry input.

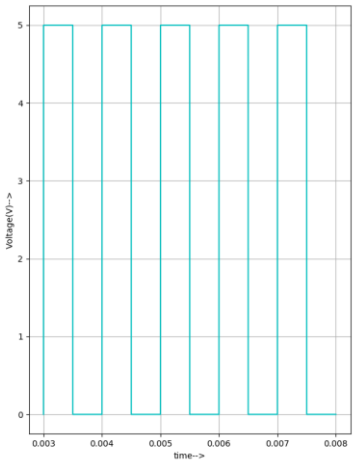

Fig. 8. Input B0

Figures 8, 9, 10 and 11 represent the four input bits of B.

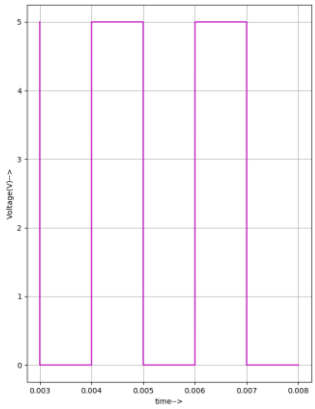

Fig. 9. Input B1

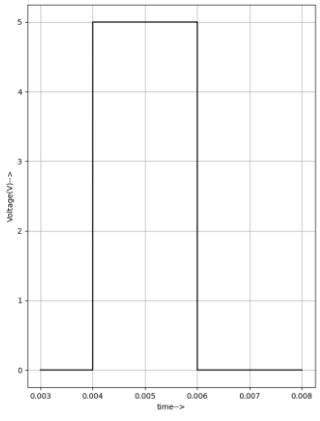

Fig. 10. Input B2

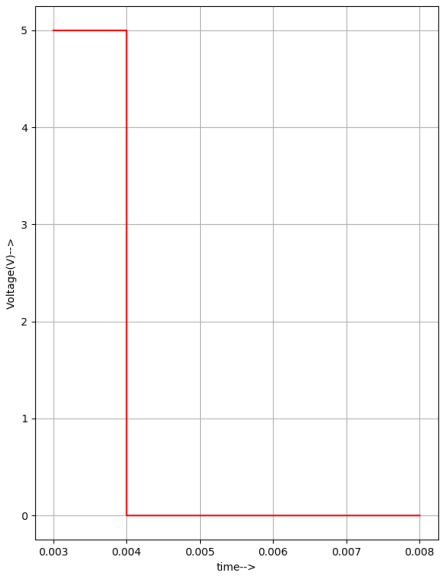

Fig. 11. Input B3

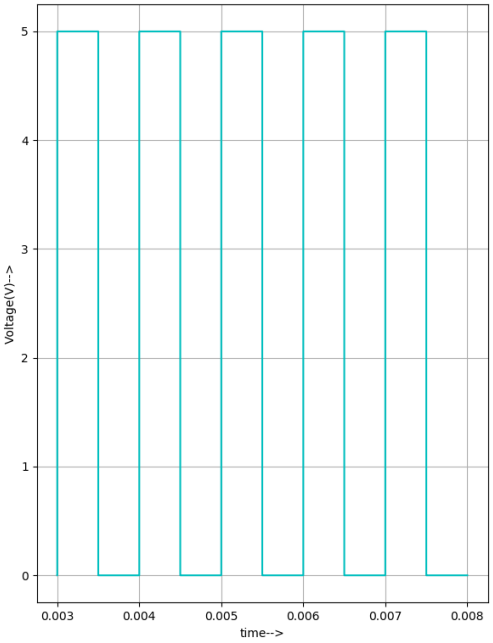

Fig. 12. Output S0

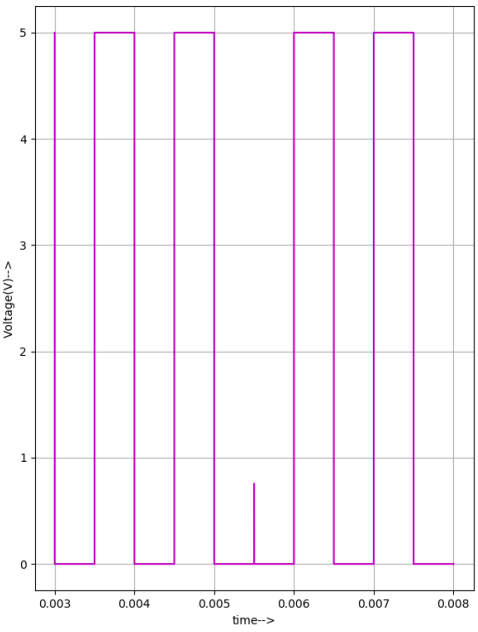

Fig. 13. Output S1

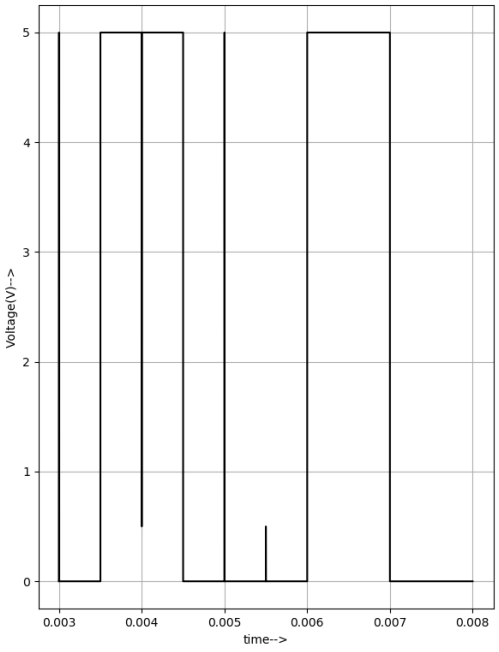

Fig. 14. Output S2

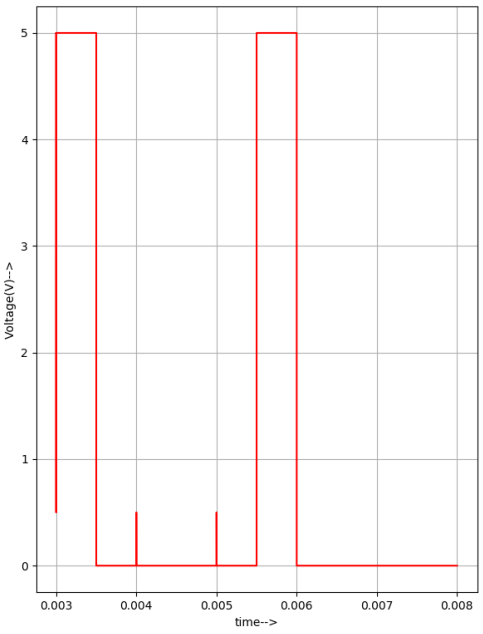

Fig. 15. Output S3

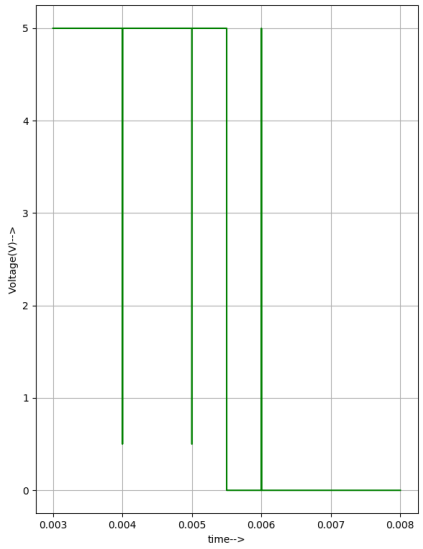

Fig. 16. Output Carry

Figures 12 to 16 represent Sum bits and Carry Out.

V. Analysis

The working of the 4-bit BCD Adder was verified using transient analysis in eSim. This analysis observed how the outputs (S0–S3, C4, and detection signal) changed over time when different input pulses for A, B, and Cin were applied. The transient analysis waveforms confirmed correct timing, proper switching of signals, and accurate generation of BCD sum and carry outputs. The timing analysis also validated the detection logic behavior during correction cycles.

VI. Conclusion

The 4-bit BCD Adder was successfully implemented in eSim using binary adders and correction logic. Transient analysis confirmed that the circuit produced correct BCD outputs (S0–S3), carry output (C4), and detection signals for different input combinations. The transient simulation results showed proper timing behavior and accurate BCD arithmetic. This design demonstrates an efficient method for decimal arithmetic in digital systems.

References

Paul, R., & Shiby, B. (2016, March). On the design of a 4-bit BCD adder. International Journal of Advanced Research in Electrical, Electronics and Instrumentation Engineering, 5(Special Issue 4). National Conference on Signal Processing, Instrumentation and Communication Engineering