Type-II - 3rd Order Phase-Locked Loop (PLL) Design

Introduction : A Phase-Locked Loop (PLL) synchronizes the phase and frequency of a generated signal with a reference signal. A Type-II, 3rd order PLL consists of a Phase Frequency Detector (PFD), Charge Pump, Loop Filter, Voltage-Controlled Oscillator (VCO), and a Frequency Divider. The PFD, designed using a NOR latch, compares the phase and frequency of the input and feedback signals, generating UP and DOWN signals. The charge pump then converts these signals into an analog current, which is further smoothed by the loop filter consisting of R1, C1, and C2. This control voltage drives a current-starved VCO, generating a corresponding output frequency. The output is divided by a factor of 48 using a divider circuit, and the feedback is compared with the reference to achieve phase lock. The Type-II, 3rd order PLL is preferred for its improved noise performance and stability. By using a third-order loop filter, the system effectively suppresses high-frequency noise. Careful design considerations, such as optimizing the loop filter components and ensuring proper biasing of the VCO, contribute to minimizing phase noise. Additionally, selecting an appropriate charge pump current and divider ratio ensures faster lock time and reliable frequency synthesis. This design is widely used in applications like clock generation, frequency synthesis, and communication systems.

Circuit Diagram :

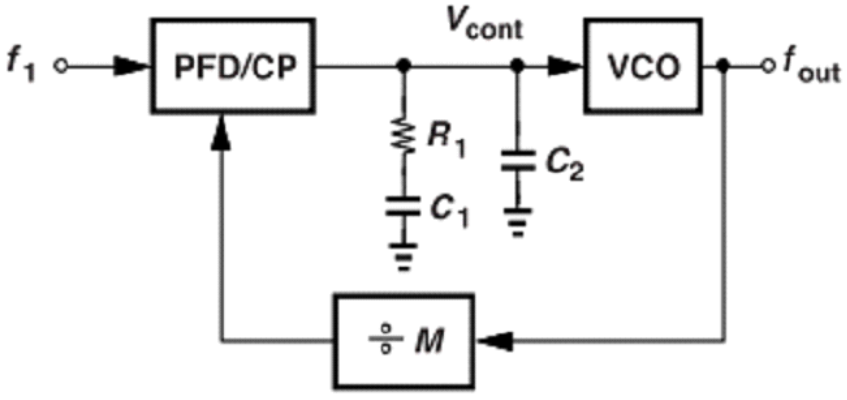

Fig - 1 : A Complete PLL (Phase Locked Loop)

Schematic :

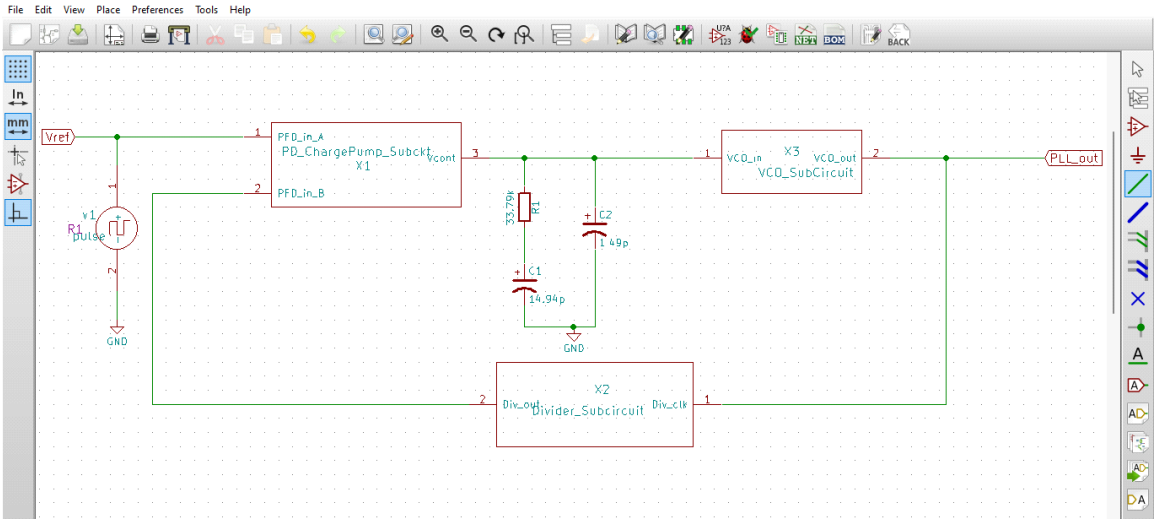

Fig - 2 : Schematic of PLL

Sub-Blocks :

1. Phase / Frequency Detector & Charge Pump

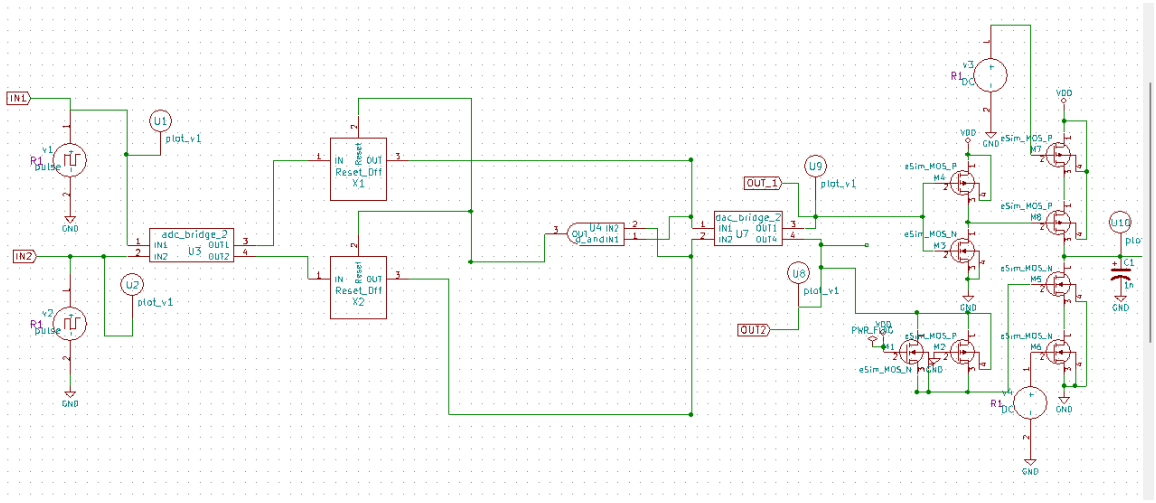

Fig-3 : Schematic of Phase Detector & Charge Pump Circuit

Output & Waveforms

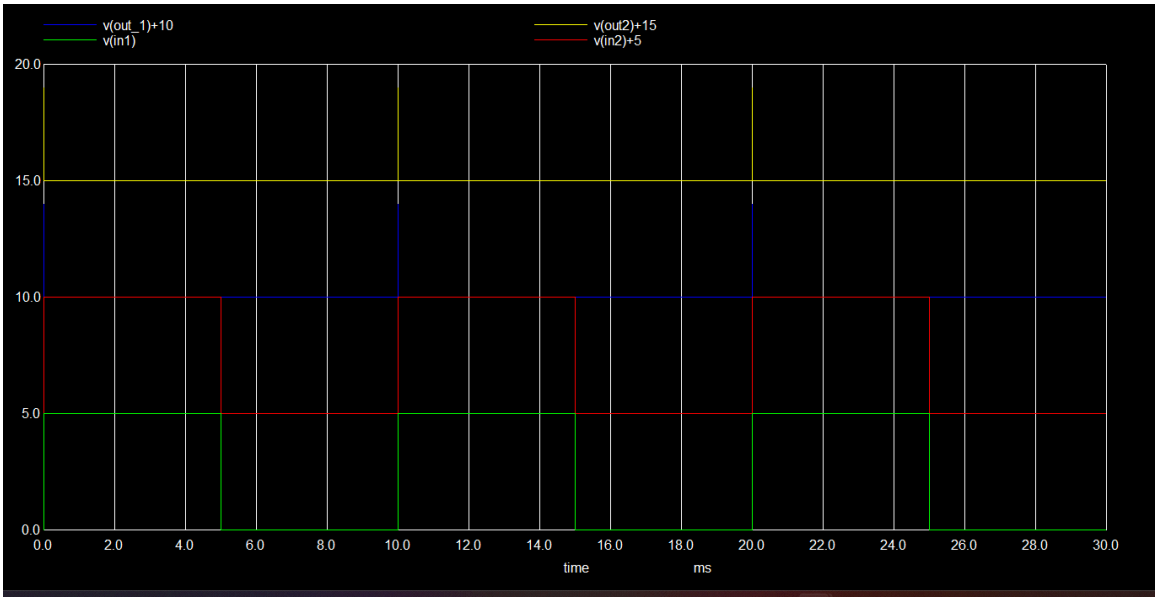

Fig-4 : Frequencies of input1 & input are equal

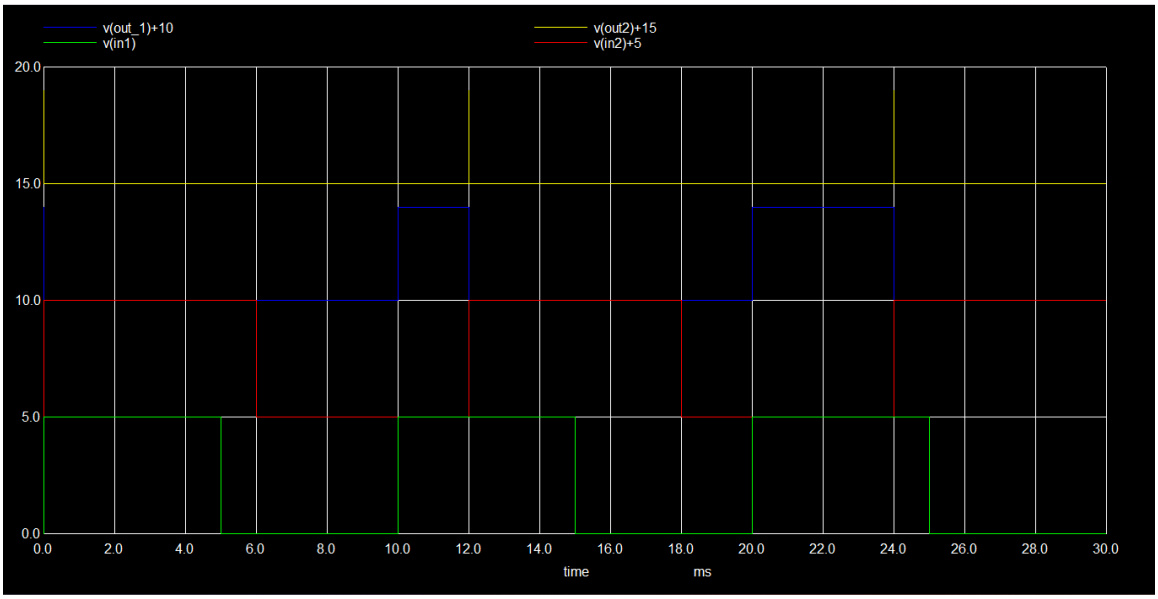

Fig-5 : Frequencies of input1 is less than input2

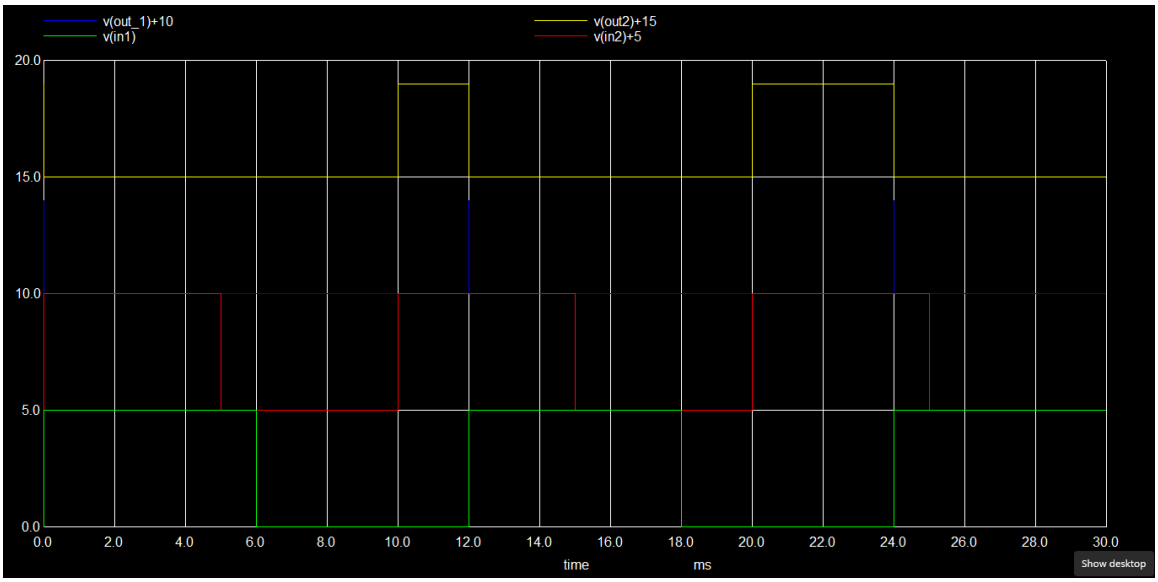

Fig-6 : Frequencies of input1 is greater than input2

2. Charge Pump

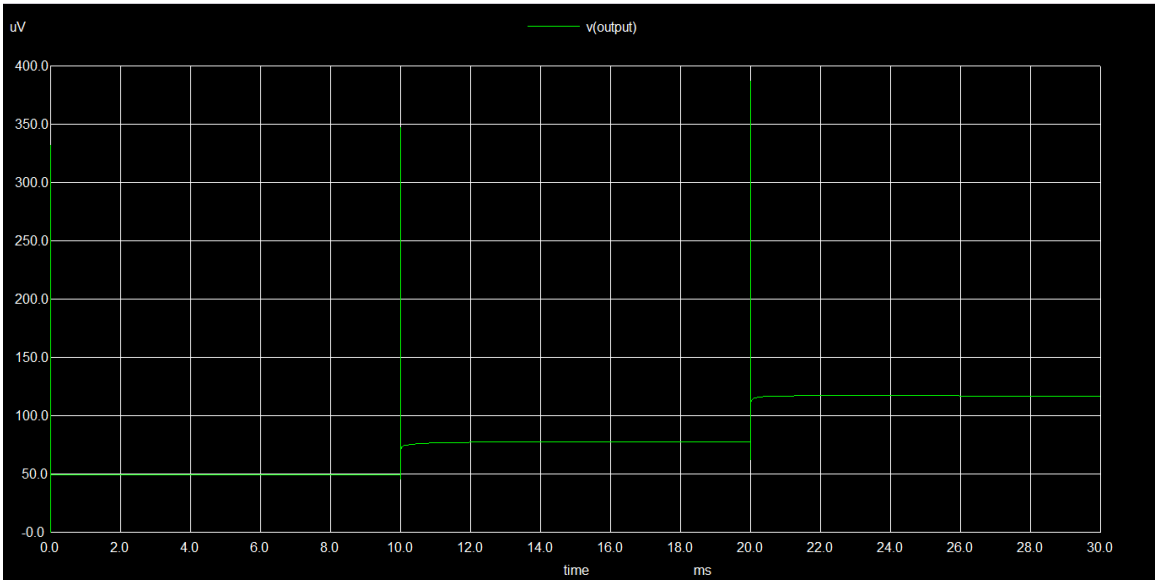

Fig-7 : Output waveform of Charge Pump

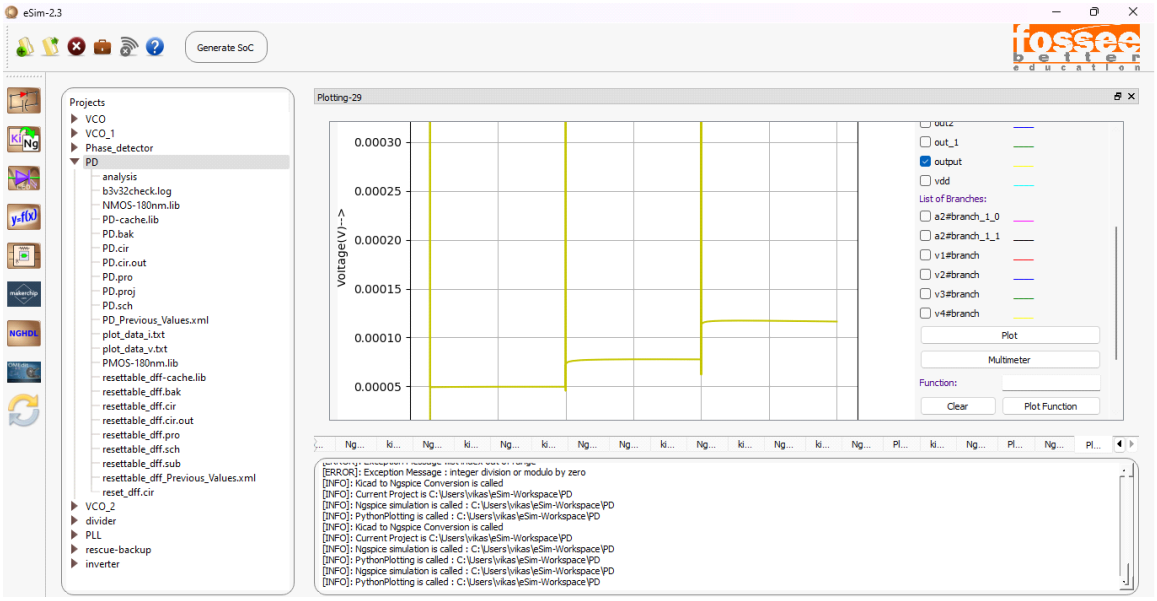

Fig-8 : Python plot of Charge Pump

3. Voltage Controlled Oscillator

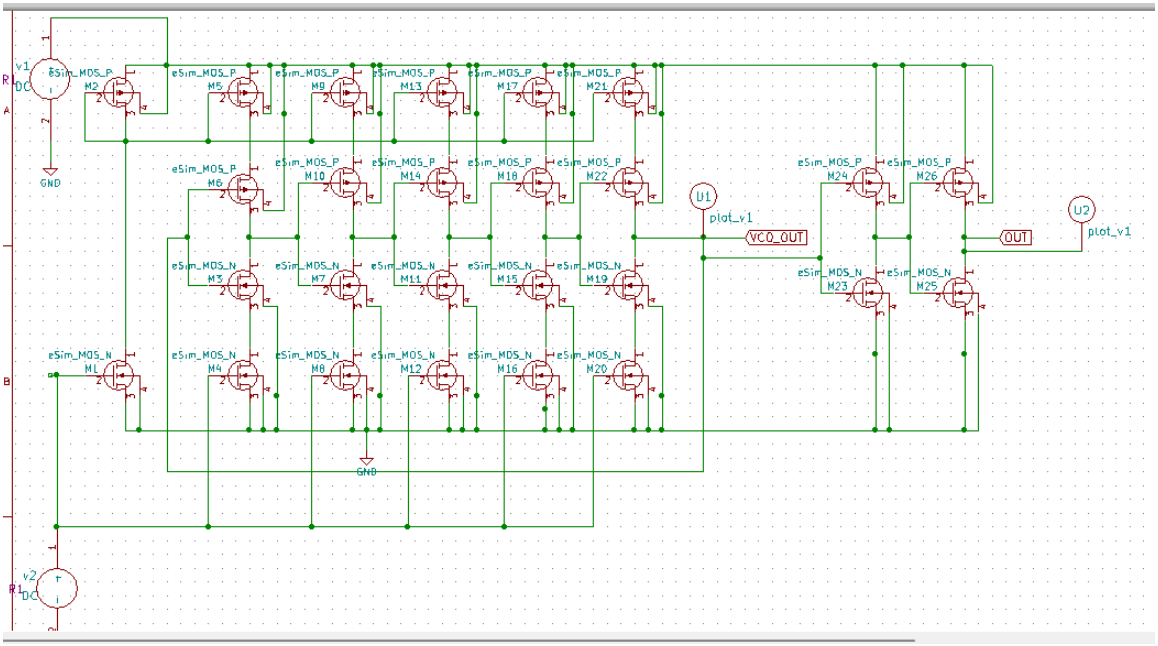

Fig - 9 : Schematic of Voltage Controlled Oscillator

Output & Waveforms

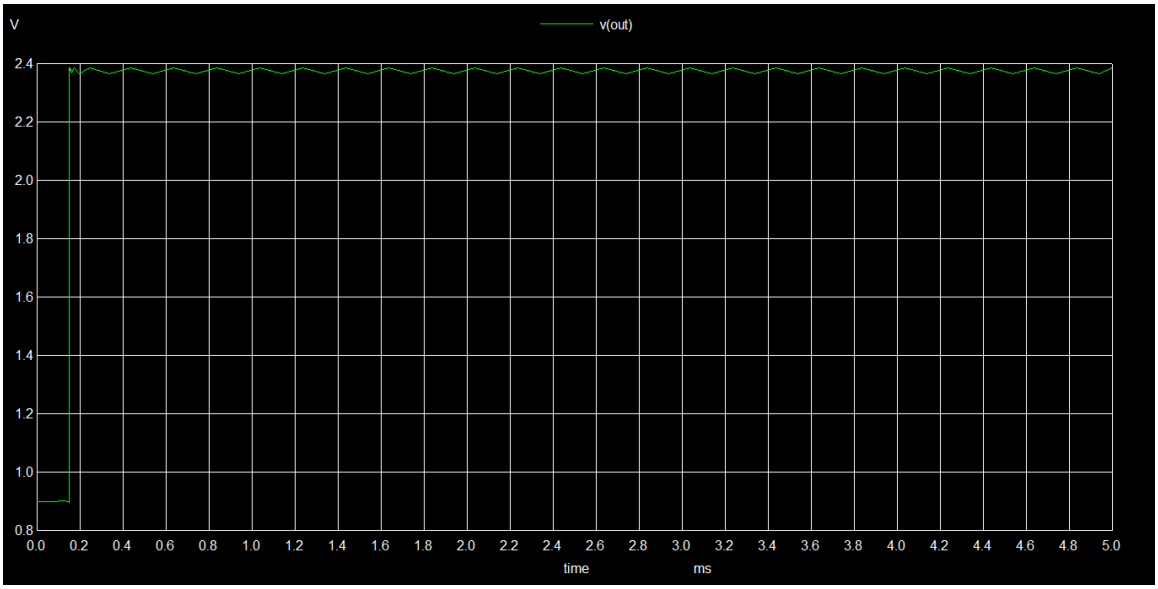

Fig-10 : Output of Voltage Controlled Oscillator

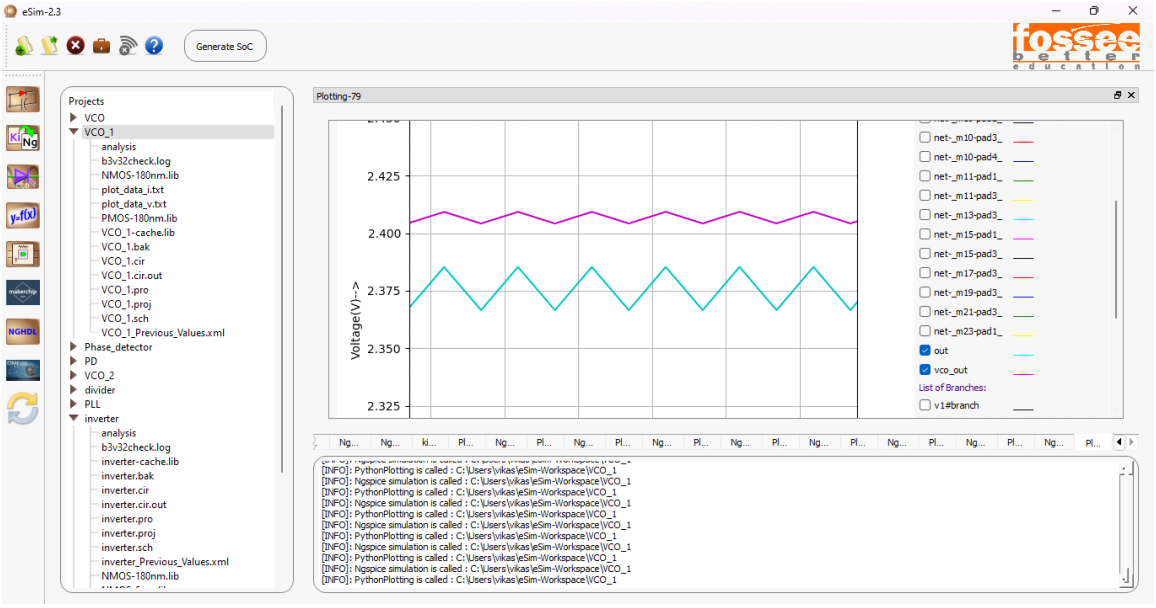

Fig-11 : Python plot of Voltage Controlled Oscillator Output

3. Divider

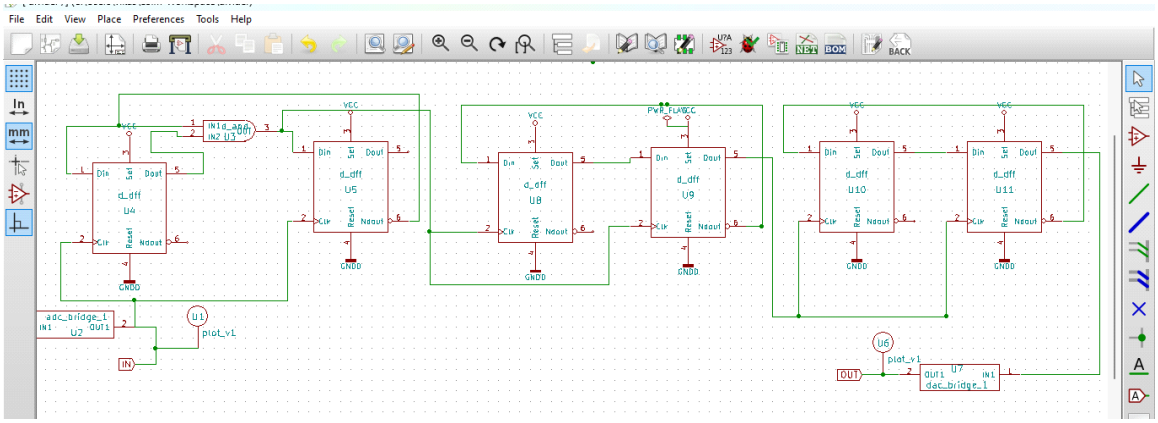

Fig - 12 : Schematic of Divider

Design the PLL : Finding R1, C1, C2, N to get fo=1.846 GHz

Given: (i) Reference frequency, fref= 38.45 MHz, (ii) fo=1.846GHz (iii) ζ=1

Use Charge pump current Ip = 100 uA, VCO Gain, KVCO = 949 MHz/V (Experimently get from VCO experiment)

$$\zeta = \frac{R_1}{2}\sqrt{\frac{I_p K_{VCO} C_1}{2\pi M}} \quad , \qquad \omega_n = \sqrt{\frac{I_p K_{VCO}}{2\pi M C_1}}. \quad , \qquad \omega_u = 2.1\omega_n = \frac{\omega_{REF}}{10}.$$

C2= 0.1 C1.

Result

From calculation, I get

C1 = 14.94 pF

C2 = 1.494 pf,

R1 = 33.79 Kohm,

Kvco = 949 MHz /V

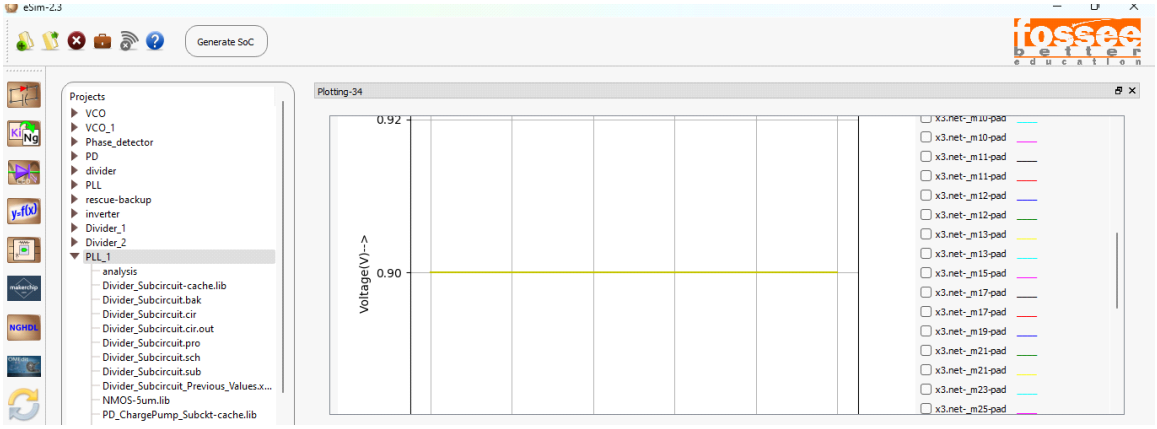

Fig-X: Output Waveform of PLL

Conclusion : Locking Achieved at = 900mv

References / Sources :

1. https://github.com/madanee20340-droid/Type-II-3rd-Order-Classical-PLL/blob/main/COMPLETE%20PLL.docx

2. https://onlinecourses.nptel.ac.in/noc22_ee92/preview

3. https://ieeexplore.ieee.org/abstract/document/10129815

4. Design of CMOS Phase-Locked Loops: From Circuit Level to Architecture Level - Behzad Razavi

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