

4 Bit Carry Bypass Adder

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Abstract— This project explains the design and working of a 4-bit Carry Bypass Adder (CBA). It adds two 4-bit binary numbers using full adders to generate the sum bits. The circuit also checks whether the carry input can pass straight through all four stages. If so, a multiplexer allows the carry to skip ahead, making the addition faster.

Keywords— Carry Bypass Adder, Carry Skip, Propagate Signal, Multiplexer

I. INTRODUCTION

A 4-bit Carry Bypass Adder is a digital circuit that performs the addition of two 4-bit numbers along with a carry input. Each stage of the adder produces a sum bit and a carry output. To improve the speed, the circuit checks if all stages are in propagate mode. When this happens, the carry does not need to move step by step but instead is directly passed to the output using a bypass path.

II. OBJECTIVES

The aim of this project is to design a 4-bit Carry Bypass Adder that can add two 4-bit numbers with a carry input. It also focuses on showing how the propagate signal lets the carry skip through the block using a multiplexer. The goal is to build the truth table, run the simulation, and confirm that the adder works as expected.

III. IMPLEMENTATION

The 4-bit Carry Bypass Adder is built using four full adders and one multiplexer. Each full adder takes two input bits and a carry input to produce a sum and a carry output. For every bit, a propagate signal is calculated as $p_i = a_i \text{ XOR } b_i$, and all four are combined to get the block propagate $p = p_0 \cdot p_1 \cdot p_2 \cdot p_3$. When $p = 1$, the multiplexer passes the input carry directly to the output carry, and when $p = 0$, the carry comes from the last full adder.

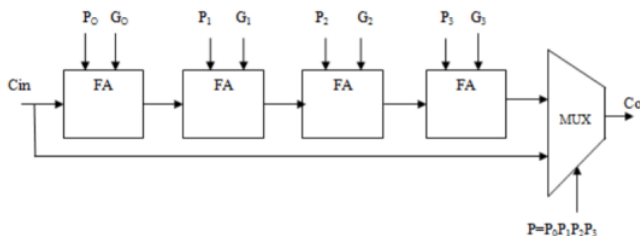


Fig. 1. Logic Diagram

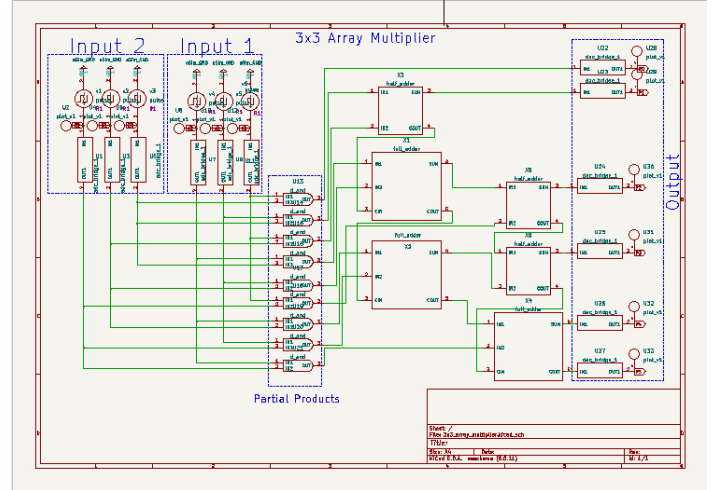


Fig. 2. eSim Circuit Schematic

IV. RESULTS

The 4-bit Carry Bypass Adder was implemented and tested. The truth table was prepared with inputs ranging from 1111 down to 0000, and the outputs of sum, carry, and propagate were verified. The results confirm that the adder performs correct binary addition for all cases. It was also observed that the propagate signal decides whether the carry is passed normally or bypassed through the multiplexer.

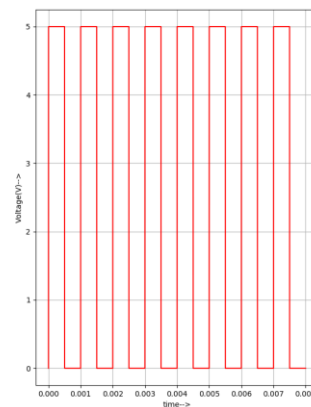


Fig. 3. Input A0

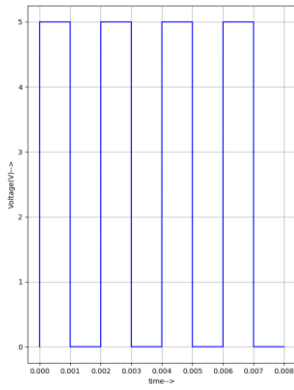


Fig. 4. Input A1

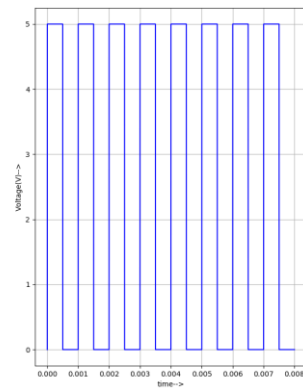


Fig. 7. Input C0

Figures 3, 4, 5, 6 and 7 represent the four input bits of A, and Carry In C0

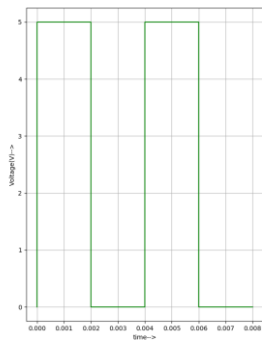


Fig. 5. Input A2

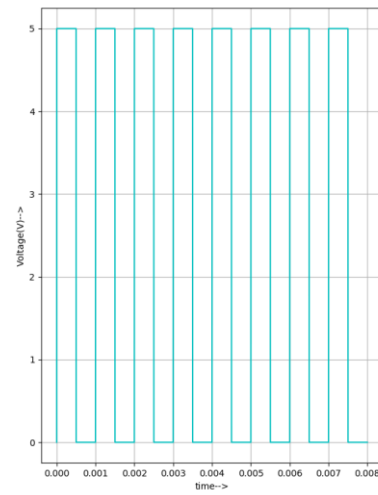


Fig. 8. Input B0

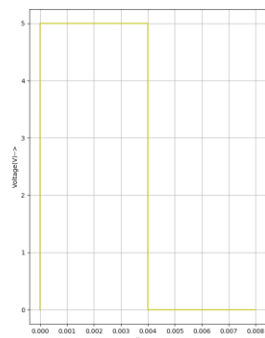


Fig. 6. Input A4

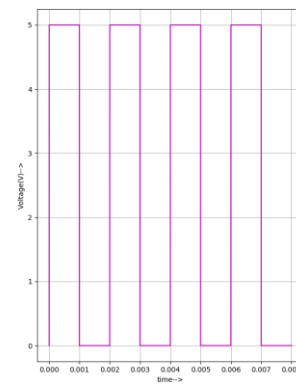


Fig. 9. Input B1

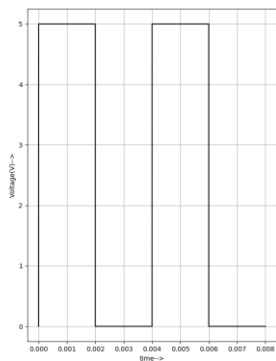


Fig. 10. Input B2

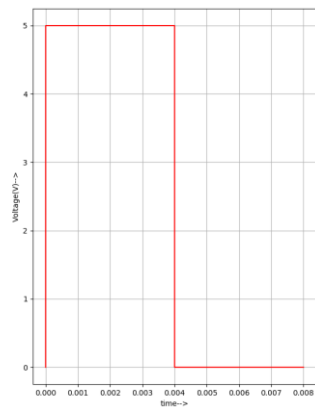


Fig. 11. Input B3

Figures 8, 9, 10 and 11 represent the four input bits of B.

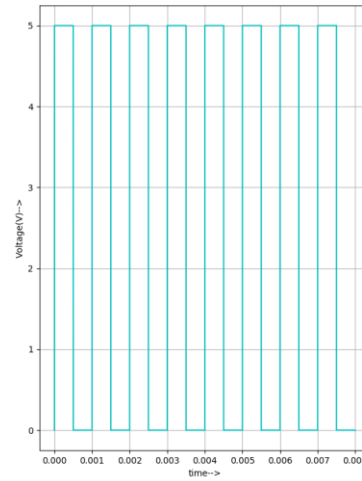


Fig. 13. Output S0

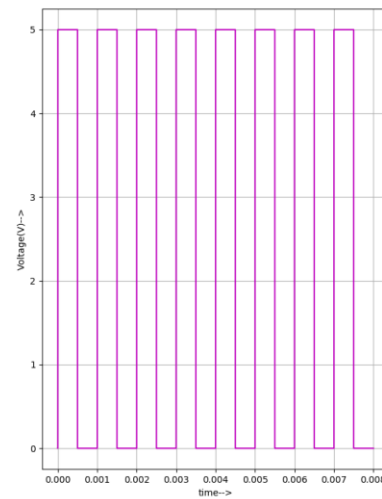


Fig. 14. Output S1

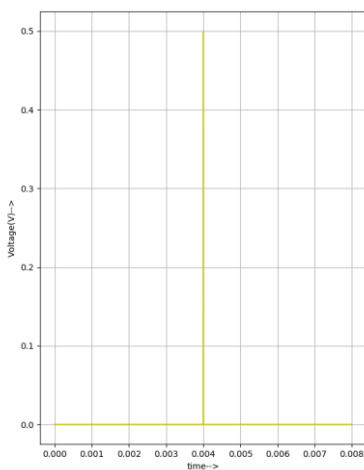


Fig. 12. Output P

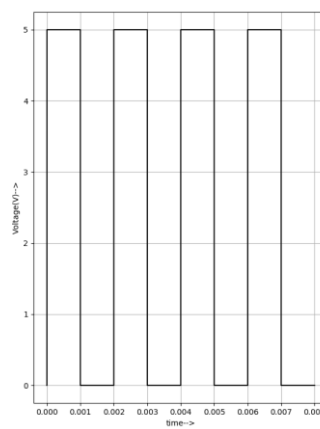


Fig. 15. Output S2

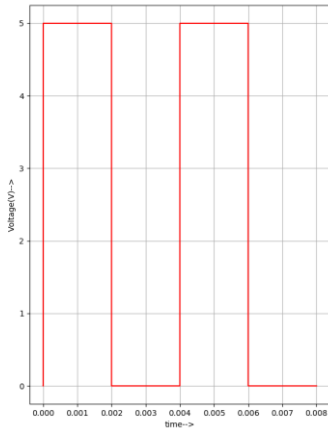


Fig. 16. Output S3

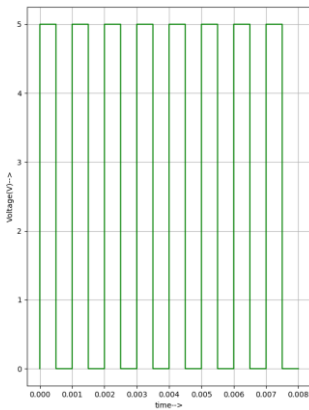


Fig. 17. Output C4

Figures 12 to 18 represent propagate bit P, Sum bits and Carry Out C4.

V. ANALYSIS

The working of the 4-bit Carry Bypass Adder was verified using transient analysis. This analysis observed how the outputs (S0–S3, C4, and P) changed over time when different input pulses for A, B, and C0 were applied. The waveforms confirmed correct timing, proper switching of signals, and the correct generation of the sum and carry outputs. They also showed how the propagate signal influences the bypassing of the carry for faster operation.

VI. CONCLUSION

The 4-bit Carry Bypass Adder was successfully implemented in eSim using full adders and a multiplexer. Transient analysis confirmed that the circuit produced the correct sum outputs (S0–S3), carry output (C4), and propagate signal (P) for different input combinations. The results showed proper timing behavior and accurate addition. This design demonstrates an efficient method of improving adder performance in digital systems.

REFERENCES

Sunitha, G. S., & Rakesh, H. M. (2017). Design and implementation of adder architectures and analysis of performance metrics. *International Journal of Electronics and Communication Engineering and Technology (IJECET)*