Circuit Simulation Project

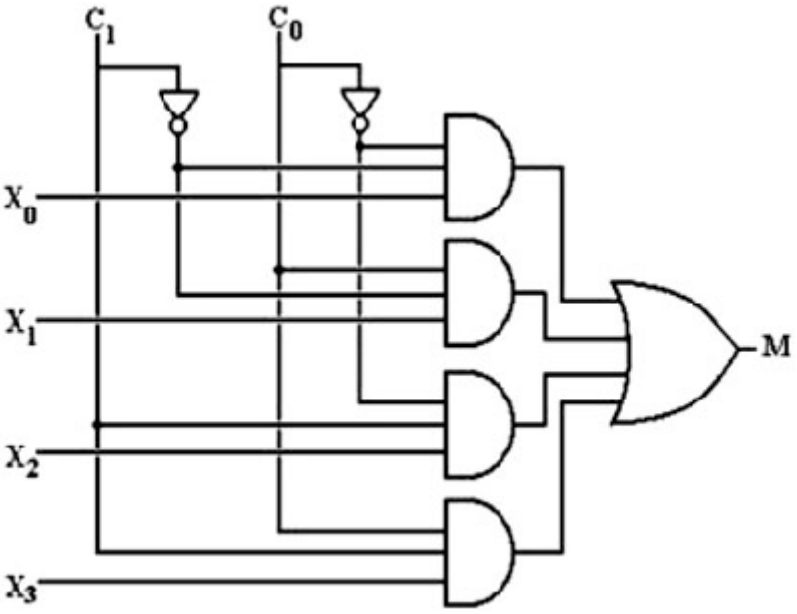
https://esim.fossee.in/circuit-simulation-project

Name of the participant : Kritish Mohapatra

Title of the circuit : 4:1 Multiplexer Design Using Logic Gates and Simulation

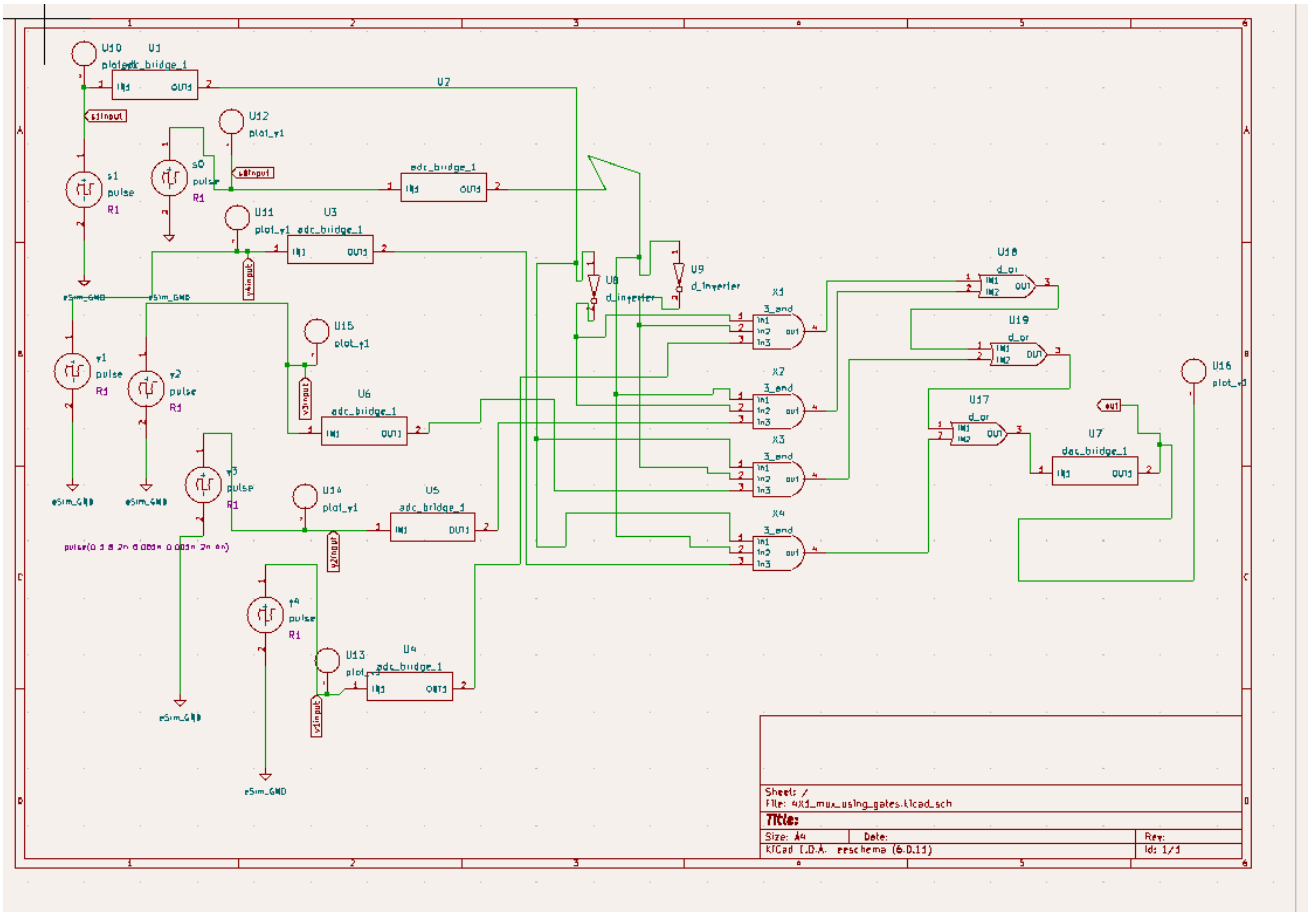
Theory/Description : The 4:1 Multiplexer (MUX) is a digital logic circuit that selects one of four input signals and routes it to a single output line based on the values of two select lines. It uses basic logic gates (AND, OR, NOT) to implement the selection function. This circuit is widely used in data routing, signal selection, and digital communication systems. The project involves designing and simulating the 4:1 MUX in eSim (KiCad + Ngspice), verifying its functionality through truth table and transient analysis, and examining practical aspects such as propagation delay and correctness of output under all input combinations.

Diagram(s) :

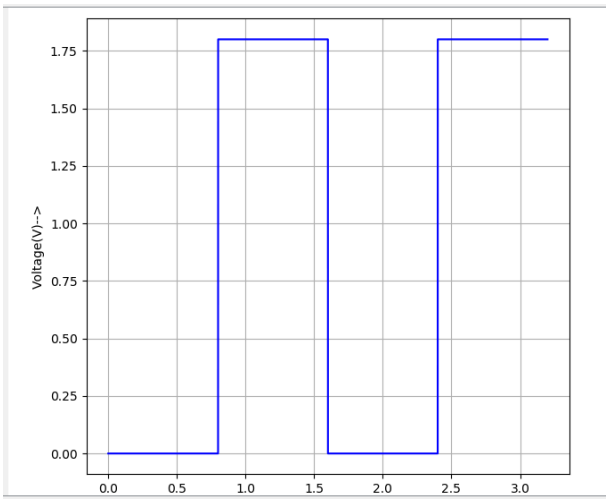


Truth Table:-

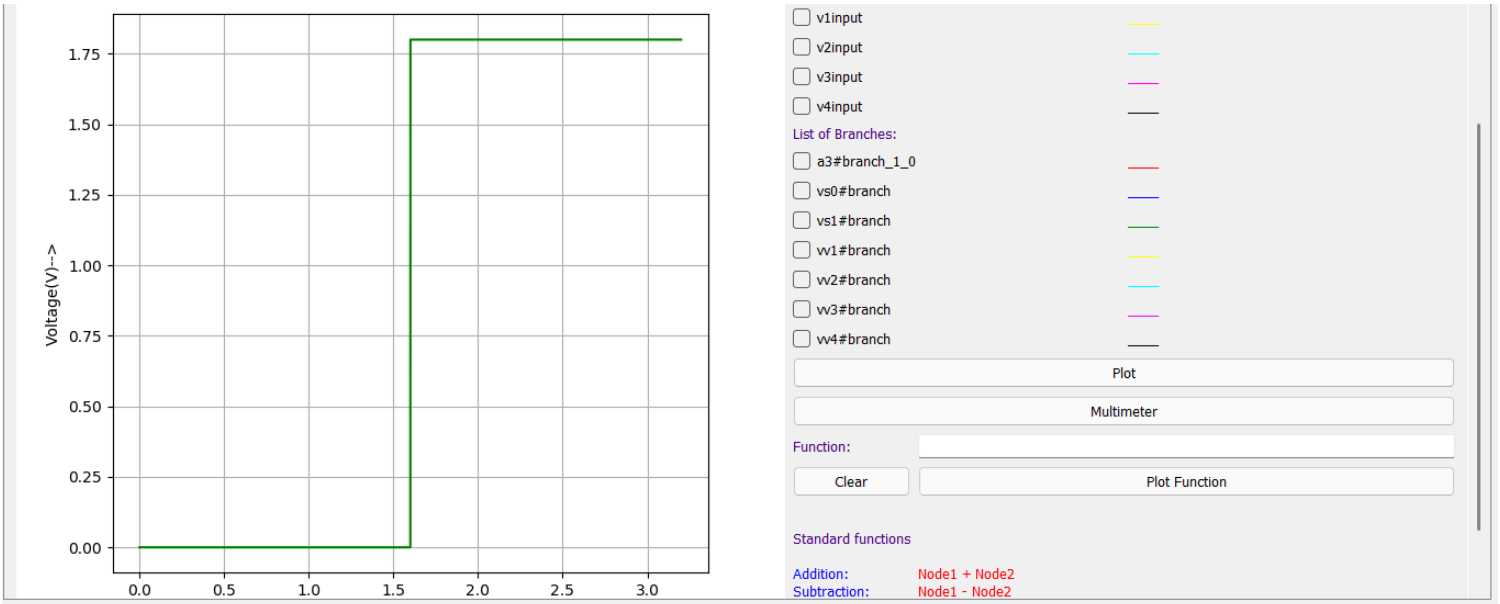
S1	S0	Y
0	0	I0
0	1	I1
1	0	I2
1	1	I3



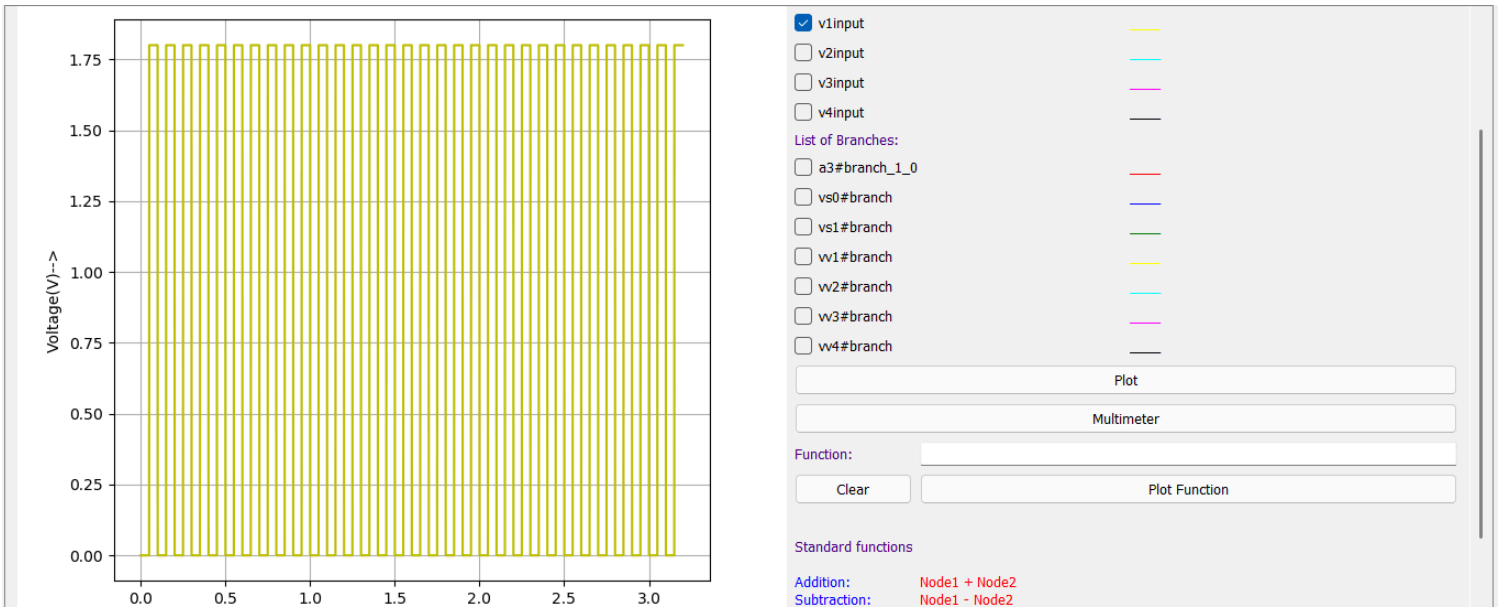
S0 wave form-:



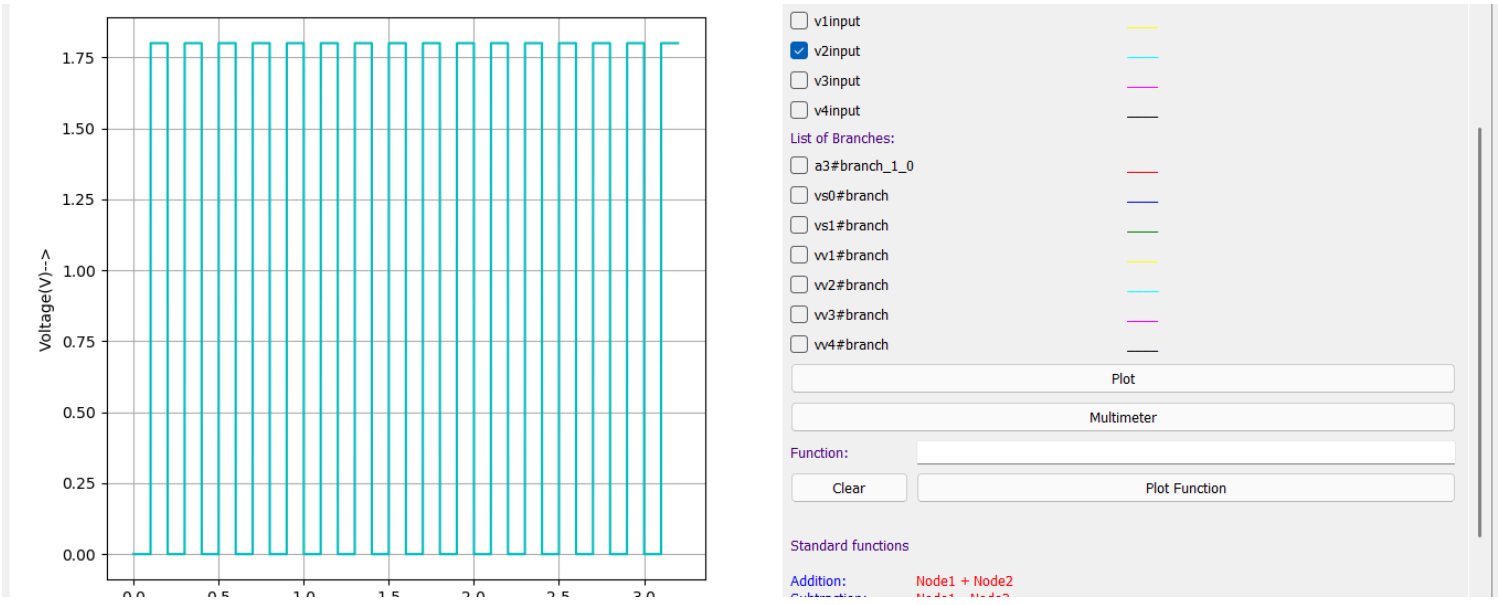
S1 wave form-



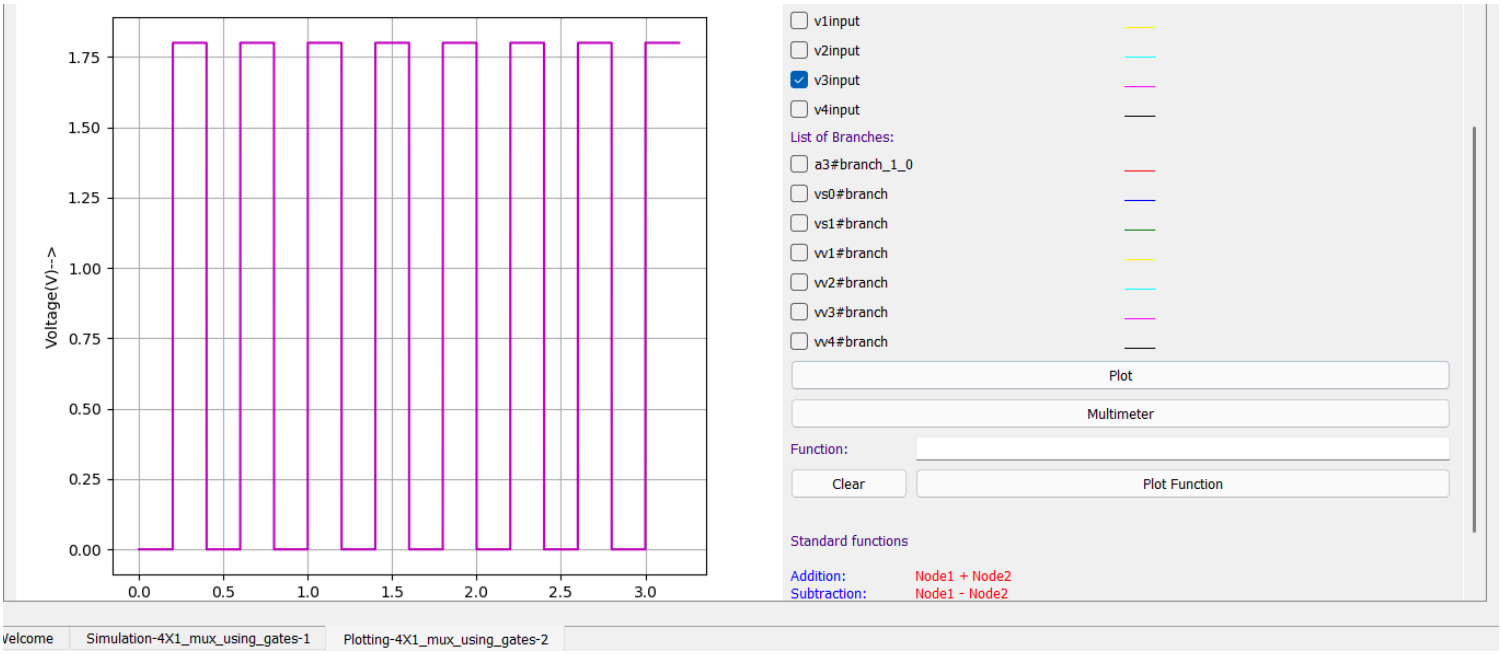
V1 waveform-



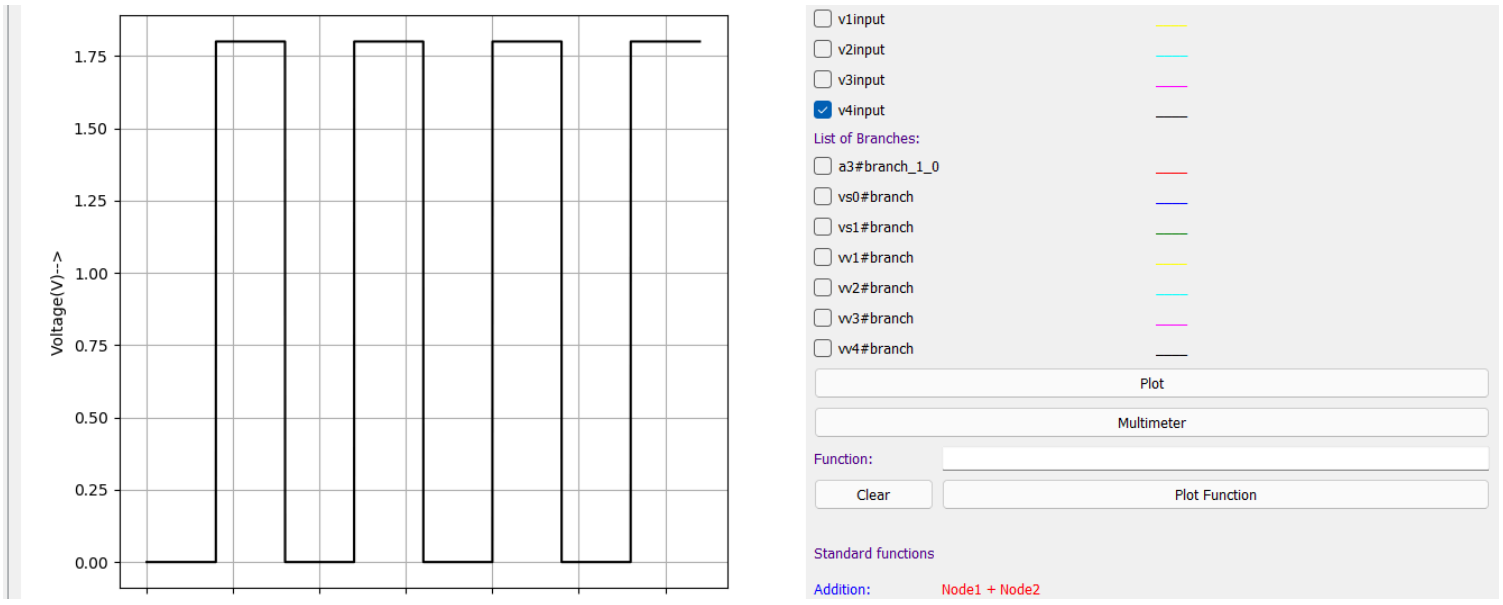
V2 wave form-



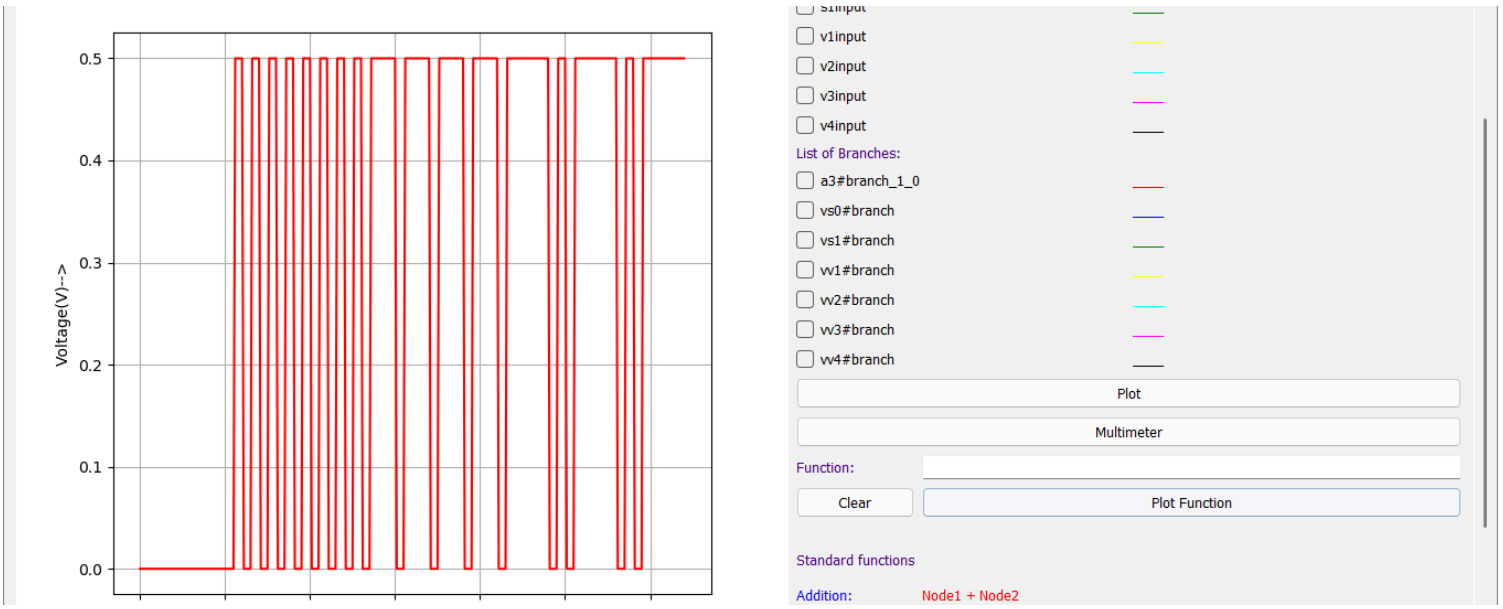
V3 waveform-



V4 waveform



Output:-



Source/Reference(s) :

https://www.researchgate.net/figure/Gate-implementation-of-a-41-Multiplexer_fig2_257799438

https://www.researchgate.net/publication/257799438_High_performance_low_power_200_Gbs_41_MUX_with_TGL_in_45_nm_technology