Report on Digital Circuit Design using eSim

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Aim : Implementation and Simulation of a 2-bit Ripple Carry Adder using CMOS Logic in eSim
(Note: Due to limited space in the work area was suppose to design 4-bit RCA but whase able to only implement 2-bit RCA)

1. Introduction

This report presents the design and simulation of fundamental digital circuits using CMOS transistor-level implementation in **eSim**. The circuits include:

- NOT Gate
- Half Adder
- Full Adder
- 2-bit Ripple Carry Adder (RCA)

These circuits form the building blocks for arithmetic and logic operations in digital systems. The project demonstrates the transistor-level design methodology, simulation setup, and functional verification using eSim.

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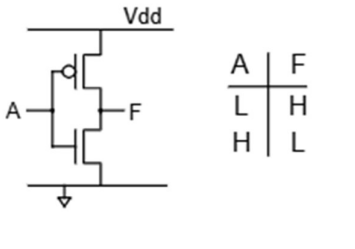
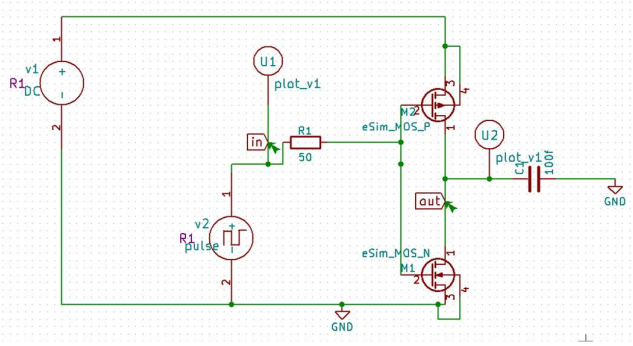
2. Circuit Design & Methodology

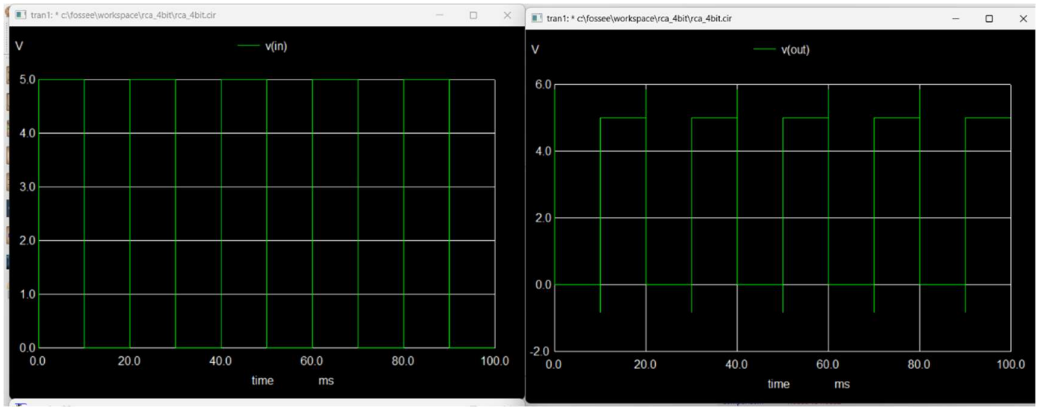
2.1 NOT Gate

- **Description**: A NOT gate (inverter) produces the complement of its input using a single PMOS and NMOS transistor in series.
- **Implementation**: Designed at transistor level using CMOS logic.



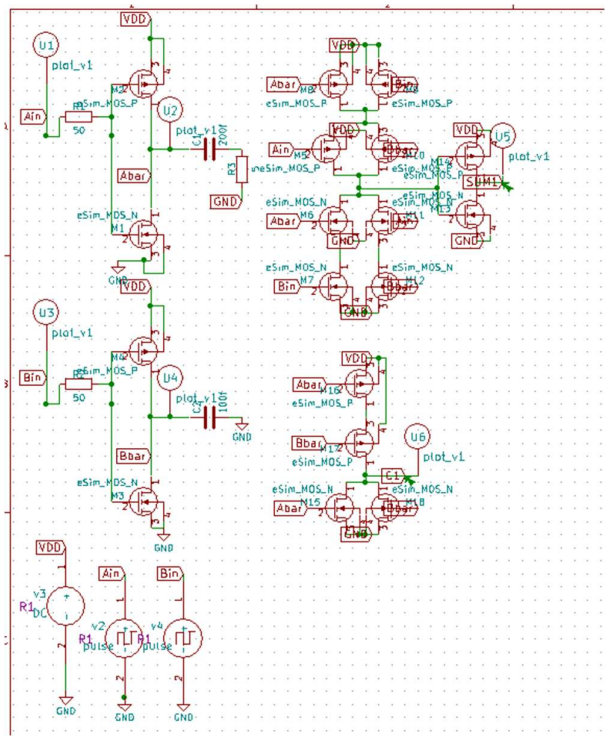


- **Simulation**: Transient analysis was performed to verify correct inversion of input.
- **Result**: Output switches between logic 0 and 1 opposite to the input.

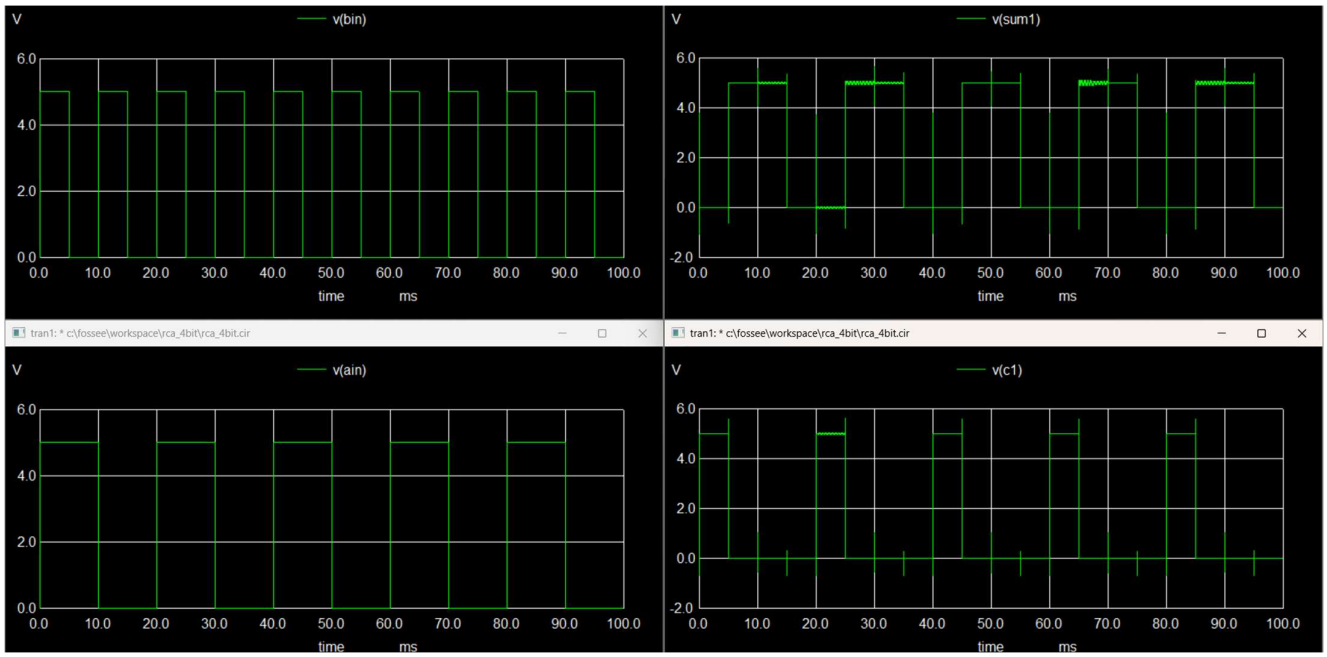


2.2 Half Adder

- **Description**: A half adder adds two single-bit binary numbers and generates **Sum** and **Carry** outputs.
- **Implementation**:
  - Sum = A $\oplus$ B (XOR gate)
  - Carry = A $\cdot$ B (AND gate)
- **Simulation**: Implemented using CMOS XOR and AND circuits.

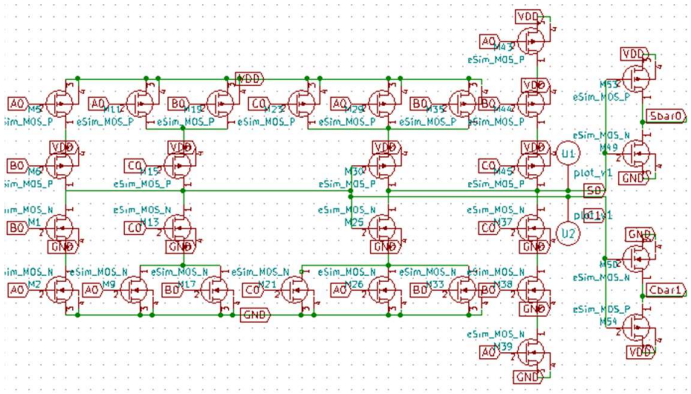


- **Result**: Truth table verified for all inputs.



2.3 Full Adder

- **Description**: A full adder adds three inputs (A, B, Cin) and generates **Sum** and **Carry** outputs.
- **Implementation**: Constructed using two half adders and an OR gate.
  - Sum = (A ⊕ B) ⊕ Cin
  - Carry = (A · B) + (Cin · (A ⊕ B))
- **Simulation**: Transistor-level realization of XOR, AND, and OR gates used.



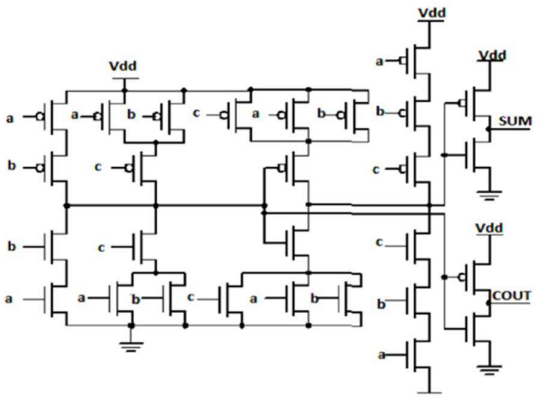
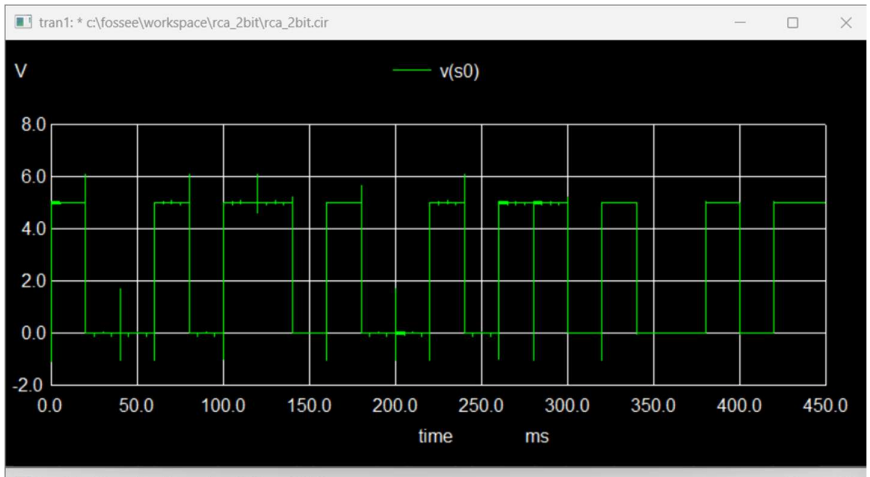
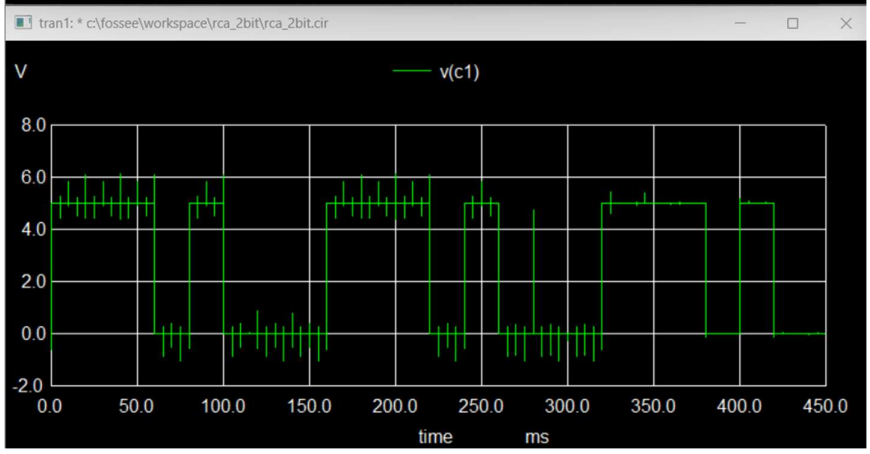


Fig 7. CMOS Full Adder

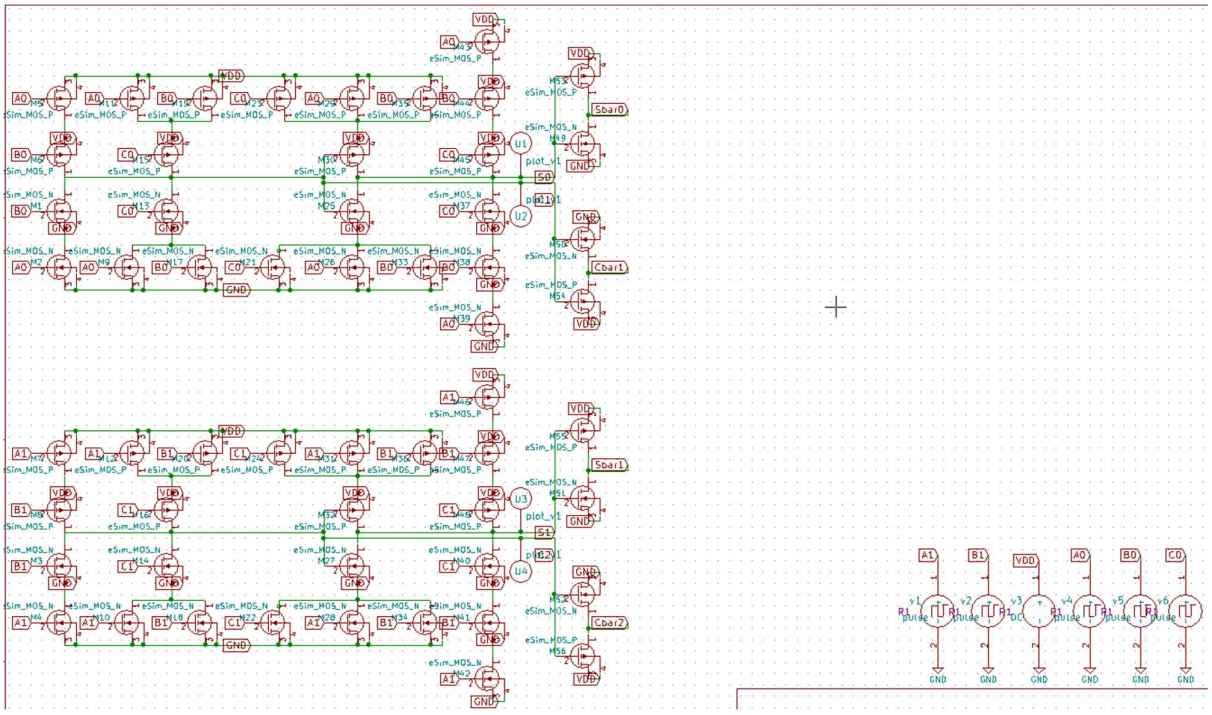
- **Result**: Verified for all 8 input combinations.



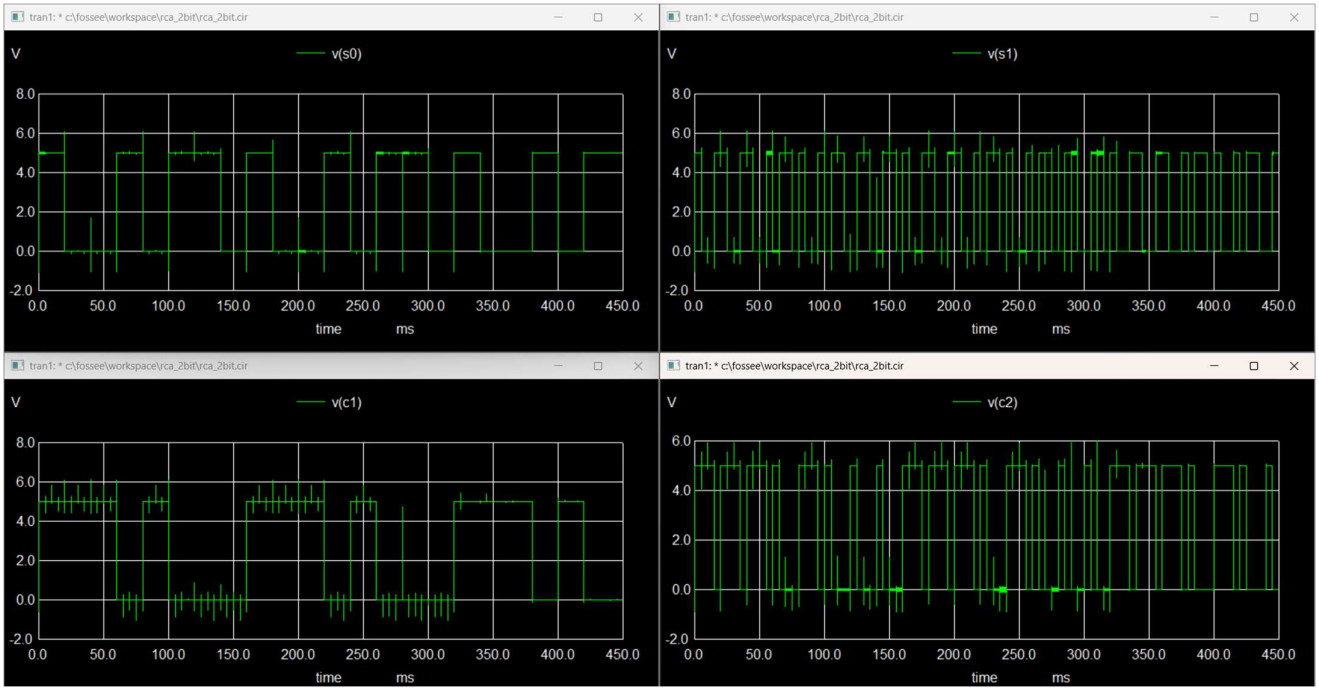


2.4 2-bit Ripple Carry Adder

- **Description**: A 2-bit RCA cascades two full adders. The carry output of the first full adder connects to the carry input of the second.
- **Implementation**: Built using two full adders from previous step.



- **Simulation**: Verified for all 4-bit input combinations (A1A0 + B1B0).
- **Result**: Correct sum and carry outputs obtained, showing ripple carry propagation.



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3. Simulation Setup

- **Tool Used**: eSim v2.3 (FOSSEE IIT Bombay)
- **Models Used**: NMOS and PMOS transistors from IHP OpenPDK of 180n Technology
- **Analysis Type**: Transient and DC analysis
- **Verification**: Waveforms captured and compared against expected truth tables

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4. Results & Discussion

- NOT gate correctly inverted inputs.
- Half adder and full adder truth tables matched theoretical results.
- The 2-bit RCA demonstrated proper addition with carry propagation.
- Minor timing delay was observed in the ripple carry path, consistent with theoretical expectations.

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5. Conclusion

The successful implementation of NOT gate, half adder, full adder, and 2-bit RCA in eSim demonstrates the capability of open-source EDA tools for digital VLSI design. This project builds a foundation for designing higher-bit adders and more complex arithmetic circuits.

6. References

1. Kumar, V., & Kumar, A. (2019). *Design and Analysis of Low Power 4-bit CMOS Ripple Carry Adder.* International Journal of Recent Technology and Engineering (IJRTE), 8(3), 2277–3878.
2. Mano, M. Morris. *Digital Design.* Pearson Education.
3. FOSSEE eSim Documentation – https://esim.fossee.in