Title of the circuit : Design and Simulation of an Inverting R-2R Ladder DAC using eSim

Theory/Description :

The proposed circuit implements an **8-bit inverting R–2R ladder Digital-to-Analog Converter (DAC)** designed to convert an 8-bit digital input word into a proportional analog voltage using a precision resistor network and an operational amplifier. The design is optimized for linearity, scalability, and ease of simulation using **eSim with ngspice**, making it suitable for mixed-signal system prototyping and verification.

The DAC operates on the **R–2R ladder architecture**, which uses only two resistor values (R and 2R) arranged in a repetitive ladder structure. Each digital input bit (D0–D7) controls a CMOS switch that connects the corresponding ladder node either to a reference voltage (Vref = -8 V) representing logic '1' or to ground representing logic '0'. This configuration generates **binary-weighted currents** corresponding to the significance of each bit, with the most significant bit contributing the highest current and the least significant bit contributing the smallest.

The ladder network is terminated at the inverting input of an operational amplifier, configured as a **current-to-voltage (transimpedance) converter**. The non-inverting input of the op-amp is grounded, creating a virtual ground at the summing node. As a result, the individual bit currents are summed linearly, and the output voltage is given by:

$$V_{out} = -V_{ref}\left(\frac{D}{2^8}\right)$$

where *D* represents the decimal value of the applied 8-bit digital input. The negative sign indicates inversion due to the inverting amplifier configuration.

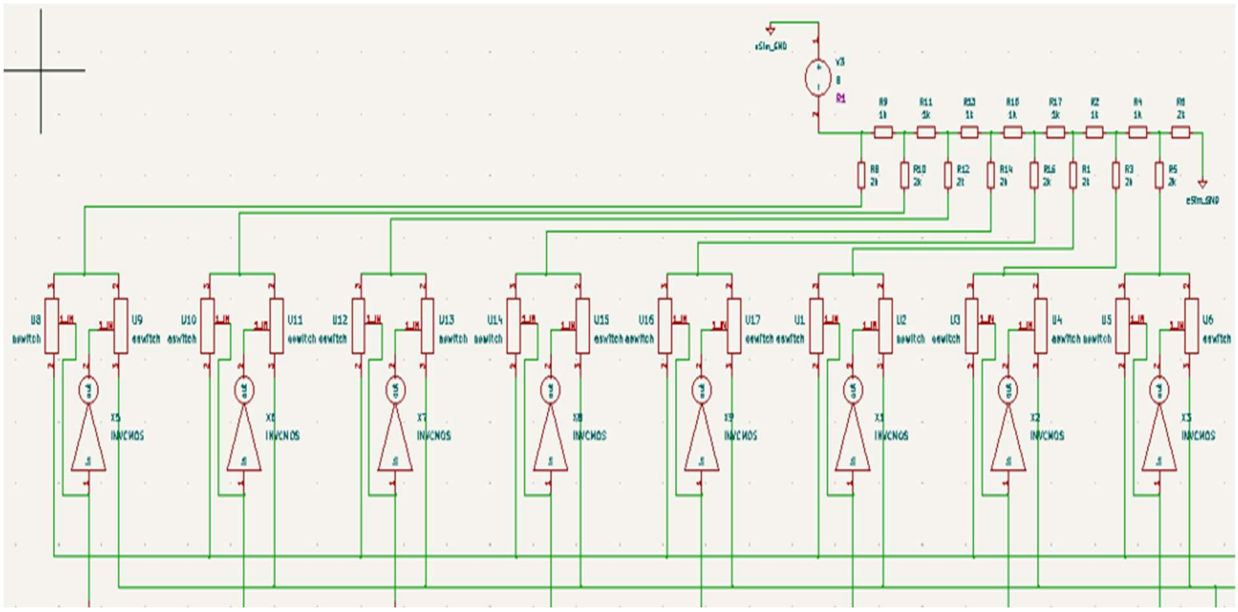
To ensure modularity and clarity, the complete R–2R ladder and switching network is implemented as a **hierarchical subcircuit** (Inverted_R_2R_DAC) within eSim. This approach improves schematic readability, enables reuse in larger mixed-signal designs, and reflects standard industry practices for complex circuit modeling.

R–2R Ladder DAC Core

• Resistor Network:
An 8-stage R–2R ladder constructed using precision resistors (R = 1 kΩ, 2R = 2 kΩ). The ladder ensures constant equivalent resistance as seen from the summing node, independent of the digital input code, which improves linearity and matching.

• Digital Switching Stage:
Each digital input (D0–D7) drives a CMOS transmission switch through inverter stages to provide clean logic-level control. The switches connect the ladder nodes to either Vref or ground, implementing binary weighting without requiring precision voltage dividers.

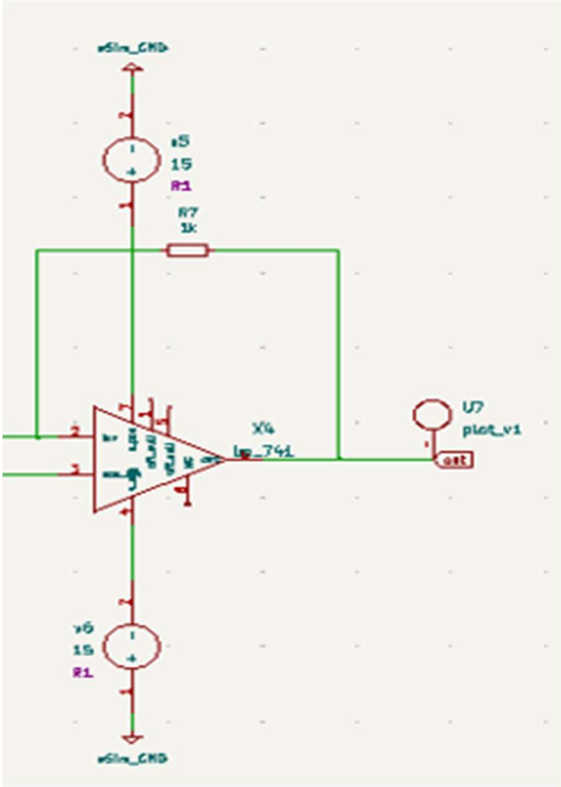
• Summing Node:
All ladder currents converge at the inverting input of the operational amplifier, which is held at virtual ground, ensuring accurate current summation.



Inverting Output Stage

• Operational Amplifier Configuration:
An LM741 operational amplifier is configured as an inverting transimpedance amplifier. The feedback resistor converts the summed ladder current into a proportional output voltage while maintaining linear operation within the supply limits (±15 V).

• Output Characteristics:
The output voltage is an inverted, continuous-time analog representation of the applied digital input. Minor output ripple observed in simulation is attributed to switch transitions, numerical convergence effects, and finite op-amp gain and bandwidth.

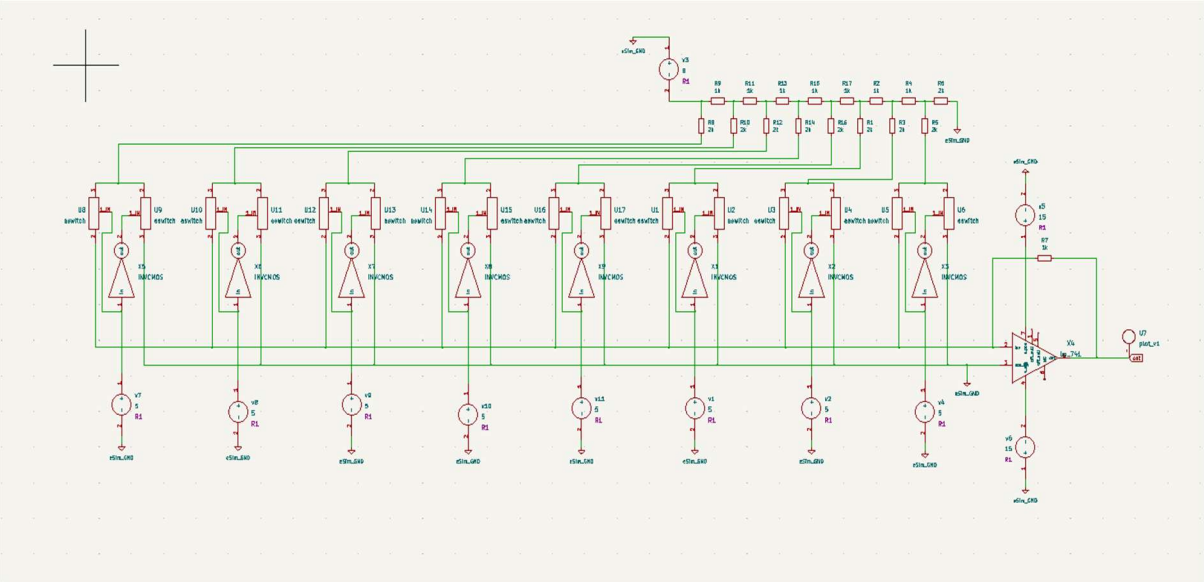


Output Waveform Characteristics

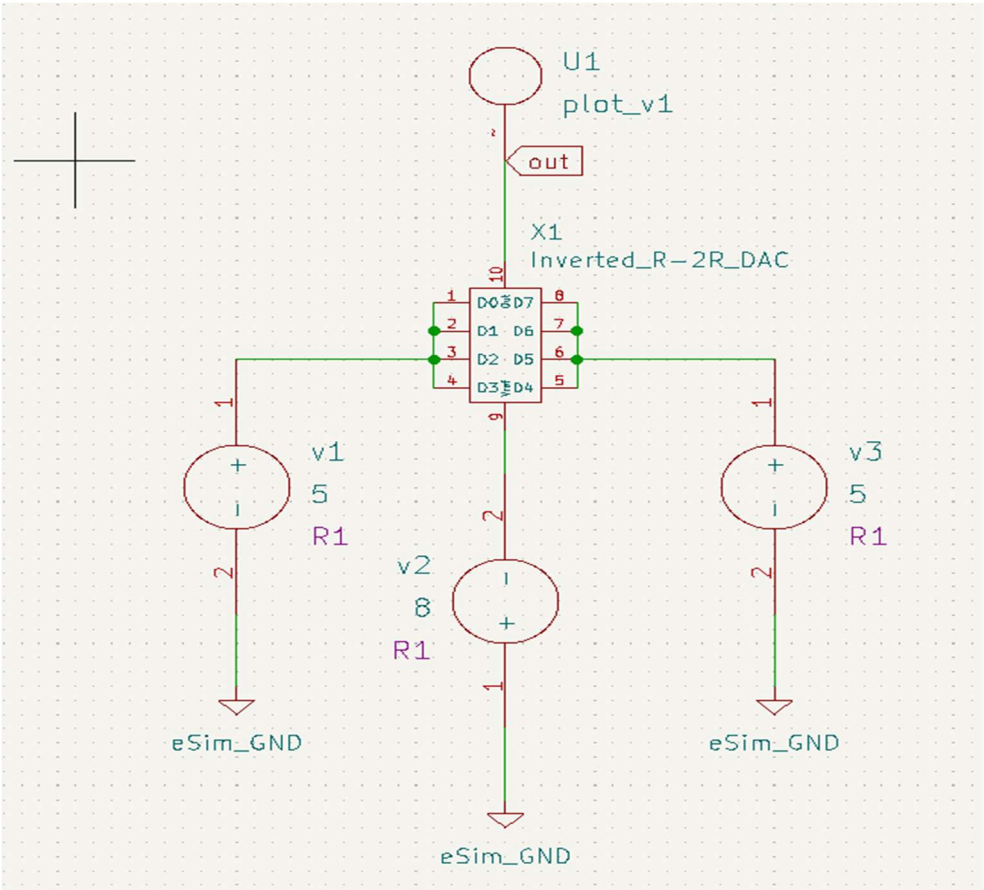
The simulated output waveform obtained from ngspice transient analysis shows a **stable DC output level** corresponding to the applied 8-bit digital input code. The measured RMS output voltage of approximately **7.97 V** confirms correct digital-to-analog conversion and validates the theoretical operation of the R–2R ladder DAC. Small-amplitude fluctuations in the waveform are consistent with practical non-idealities and do not affect functional correctness.

Circuit Diagrams :

Inverted R-2R DAC Ladder:



Test Circuit:

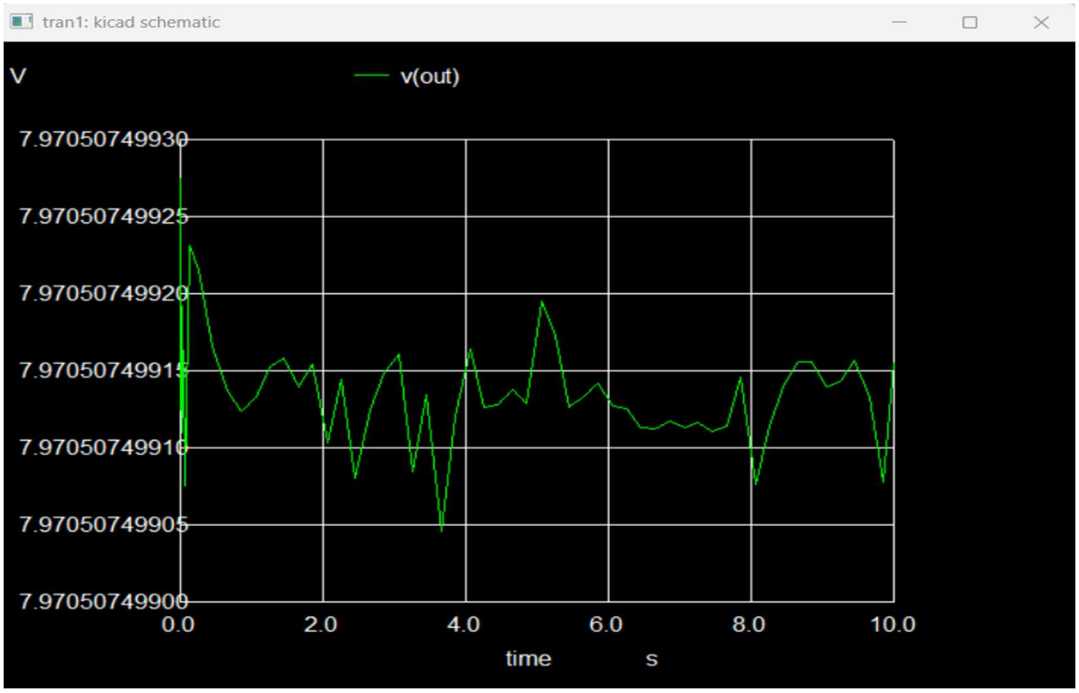


Results/ Output:

The 8-bit inverting R–2R ladder DAC was simulated using **ngspice through the eSim environment** to verify correct digital-to-analog conversion, linearity, and steady-state behavior. Transient analysis was performed while applying fixed digital input combinations to the ladder through CMOS switching stages.

Output Voltage Waveform

The output voltage waveform observed at node **out** exhibits a **stable DC level** corresponding to the applied 8-bit digital input code. After an initial settling period, the output converges to a constant value with **small-amplitude ripple**. This ripple arises from CMOS switching transitions, numerical convergence effects in SPICE simulation, and the finite gain-bandwidth product and input offset characteristics of the LM741 operational amplifier.

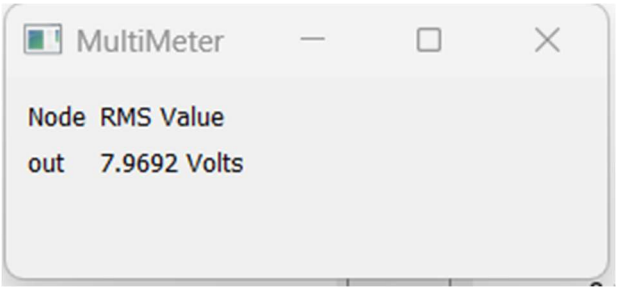


Measured Output Value

Using the eSim multimeter measurement block, the output voltage was measured in RMS mode. For the applied full-scale digital input condition, the DAC produced an output voltage of approximately:

- **Vout,RMS ≈ 7.97 V**

This measured value closely matches the expected theoretical output for an 8-bit inverting R–2R DAC operating with a 5 V reference and confirms proper current summation and voltage conversion.



Source/Reference(s) :

[1] **R. Jacob Baker**, *CMOS: Circuit Design, Layout, and Simulation*, 3rd Edition, Wiley-IEEE Press, 2019.
(Reference for R–2R ladder DAC architecture and current-mode DAC principles)

[2] **A. S. Sedra and K. C. Smith**, *Microelectronic Circuits*, 7th Edition, Oxford University Press, 2014.
(Operational amplifier modeling and inverting transimpedance configurations)

[3] **Paul R. Gray, Paul J. Hurst, Stephen H. Lewis, Robert G. Meyer**, *Analysis and Design of Analog Integrated Circuits*, 5th Edition, Wiley, 2009.