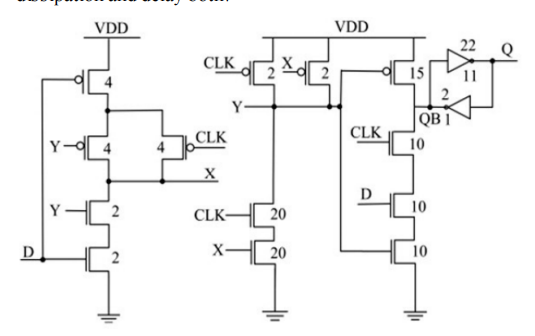
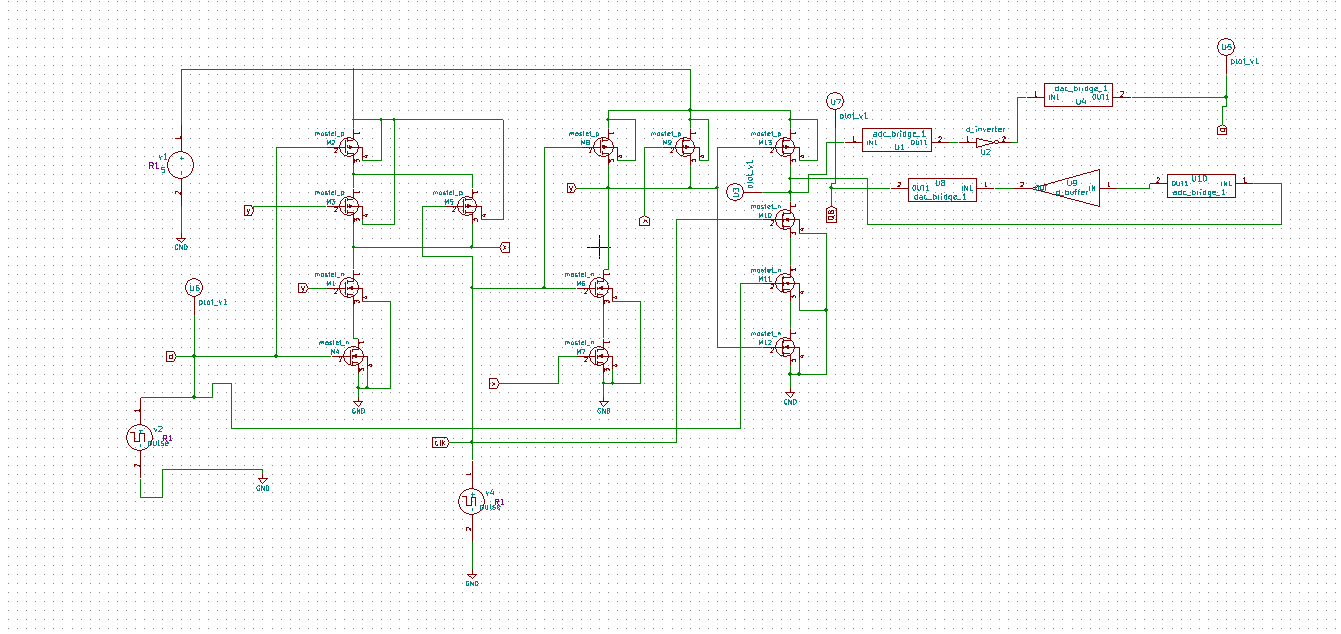
**PULSE GENERATOR LATCH BASED FLIPFLOP**

**ABSTRACT**

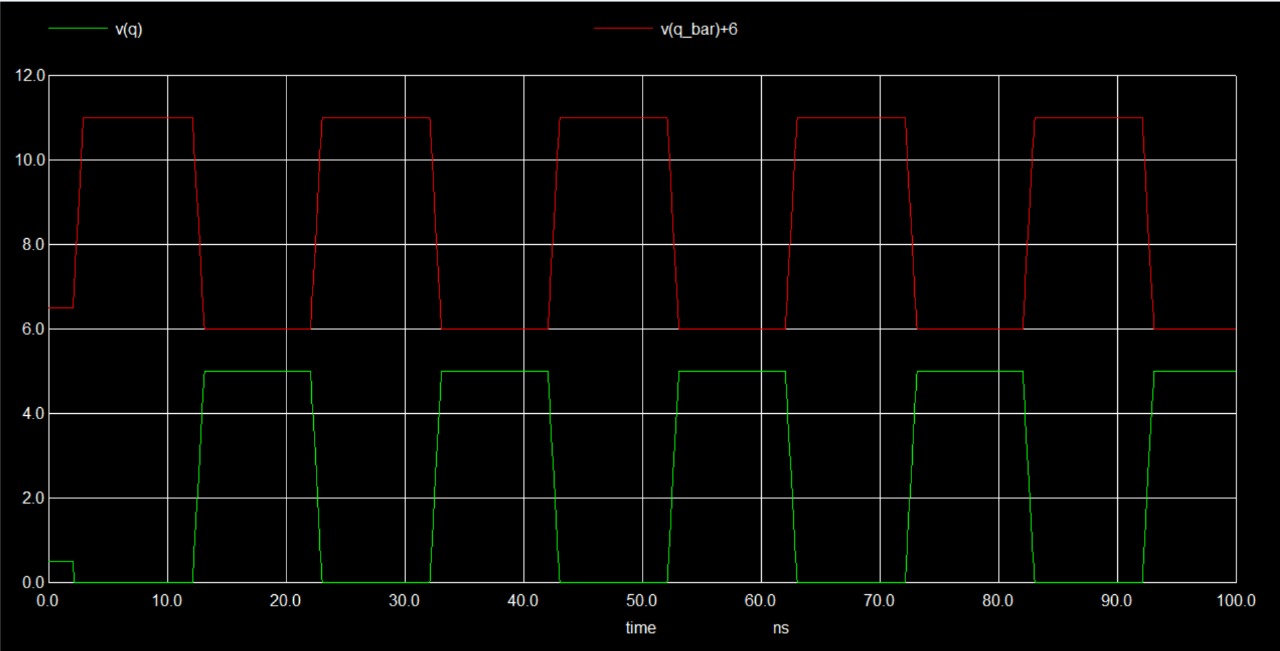
This work evaluates six advanced pulse-triggered flip-flop (P-FF) designs—CPN-LCFF, PHLFF, DDFF, XCFF, CC-LCFF, and SCCER—using 32 nm CMOS technology in SPICE simulations. The study compares power consumption and delay across voltage and temperature variations. Results show that SCCER achieves superior power efficiency, while DDFF demonstrates the best speed performance. Overall, SCCER provides the lowest power–delay product (PDP), and CPN-LCFF performs the worst.

**BLOCK DIAGRAM**

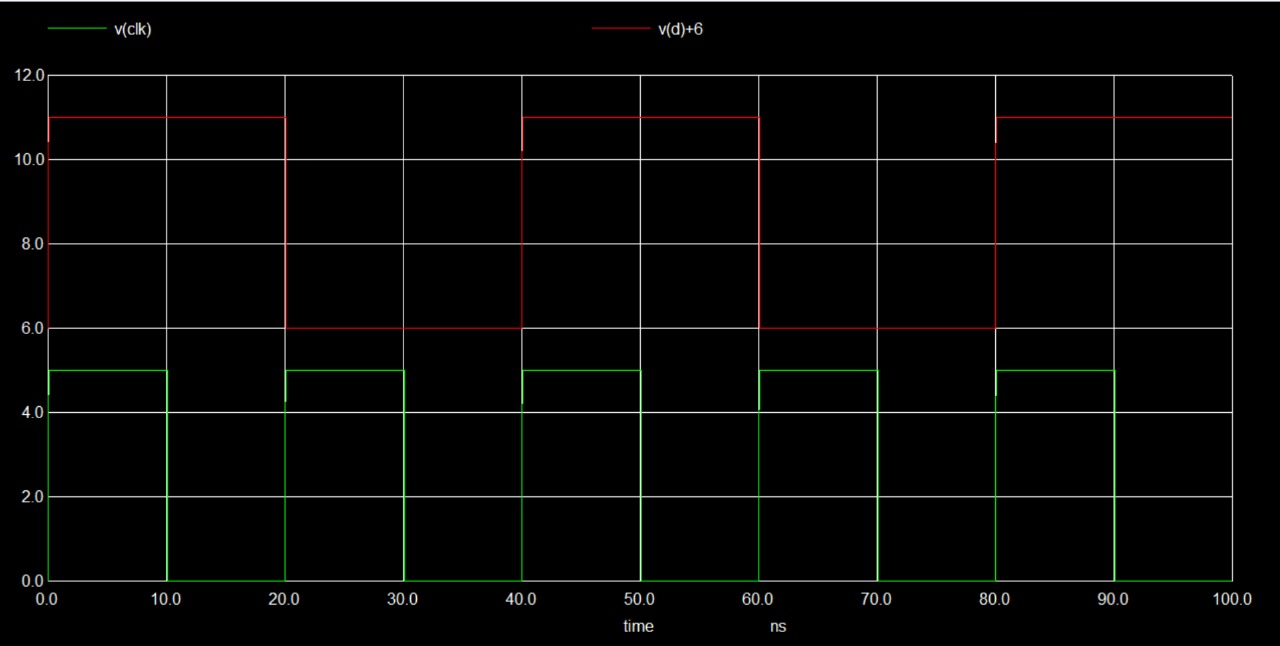
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3. **SCHEMATIC DIAGRAM **

4**. OUTPUT WAVEFORMS**



5**. INPUT WAVEFORMS**



**References:**

[1] https://ieeexplore.ieee.org/document/10141264

[2] <https://doi.org/10.1109/ICACCCN.2018.8748364>

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