Circuit Simulation Project

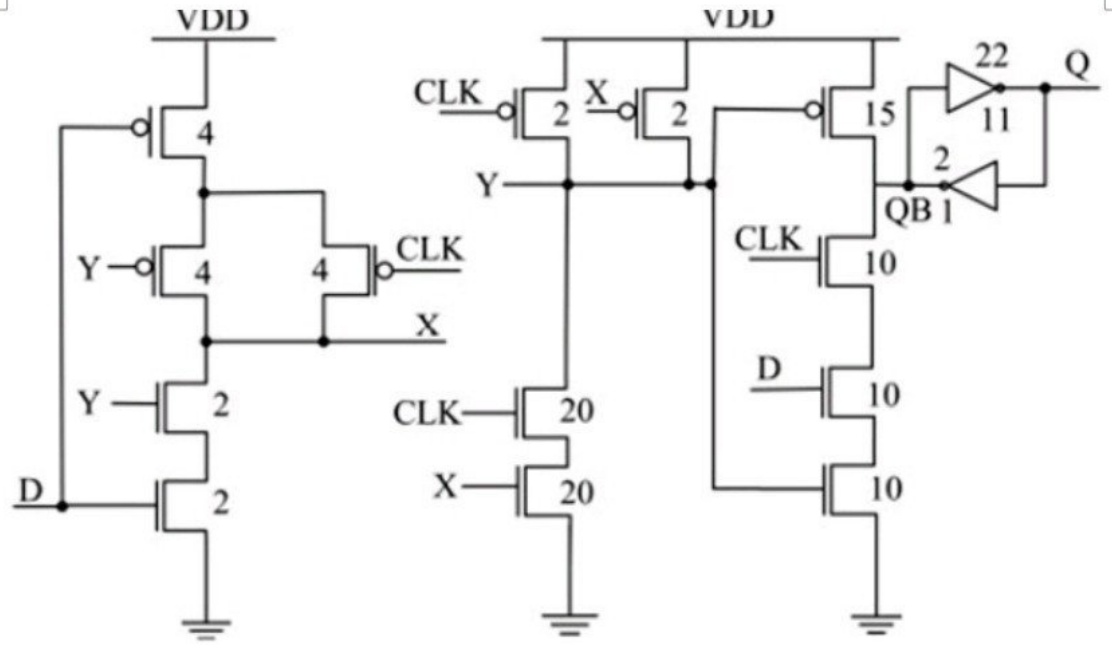
https://esim.fossee.in/circuit-simulation-project

Name of the participant: S.Pandiyarajan

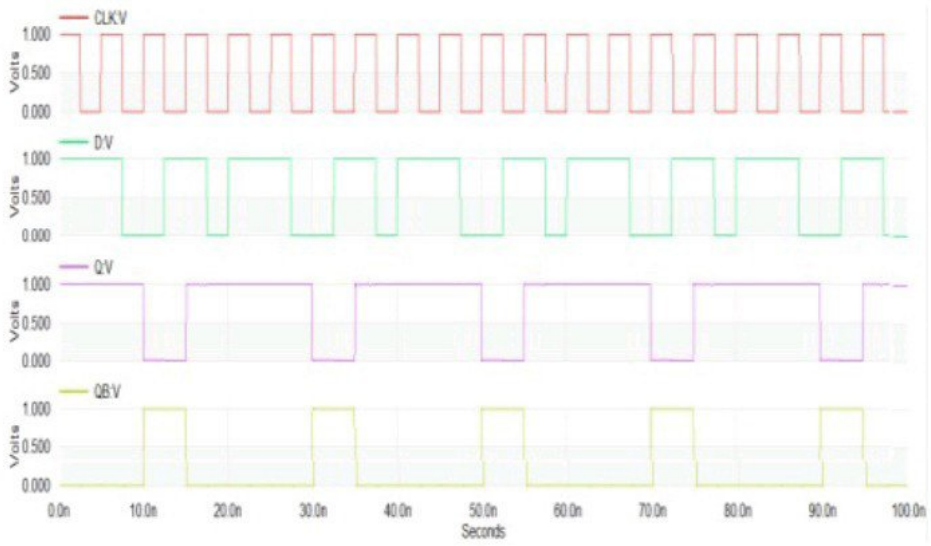
Title of the circuit: Pulse Generator Free Hybrid Latch based Flip Flop using Esim

Theory/Description: Flip-flops (FFs) are critical storage elements in CMOS circuits and microprocessors, but they contribute significantly to power consumption, with clock networks consuming nearly 50% of total system power. To address this, pulse-triggered flip-flops (P-FFs) are preferred over conventional master-slave FFs due to their simpler design, reduced power usage, and high-speed performance. P-FFs require only a single latch and can tolerate clock jitter while saving chip area and energy. They are categorized into implicit and explicit types, based on pulse generation methods. This work compares six advanced P-FF designs under varying voltages and temperatures, analyzing their delay and performance trade-offs. The study highlights P-FFs as efficient candidates for low-power, high-performance CPU architectures.

Circuit Diagram(s)



Results (Input, Output waveforms and/or Multimeter readings) :



Source/Reference(s):

Title of the Paper: Performance Evaluation of Pulse Triggered Flip flops in 32 nm CMOS Regime

Name of the journal/Publication: IEEE Solid State Circuits

Author(s): Jinn-Shyan Wang, Po-Hui Yang, and Duo Sheng

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LINK: https://ieeexplore.ieee.org/document/10141264