

Research Migration Project

Title: Design and Analysis of a StrongARM Latch Comparator Using eSIM

Participant: Karthigaa S

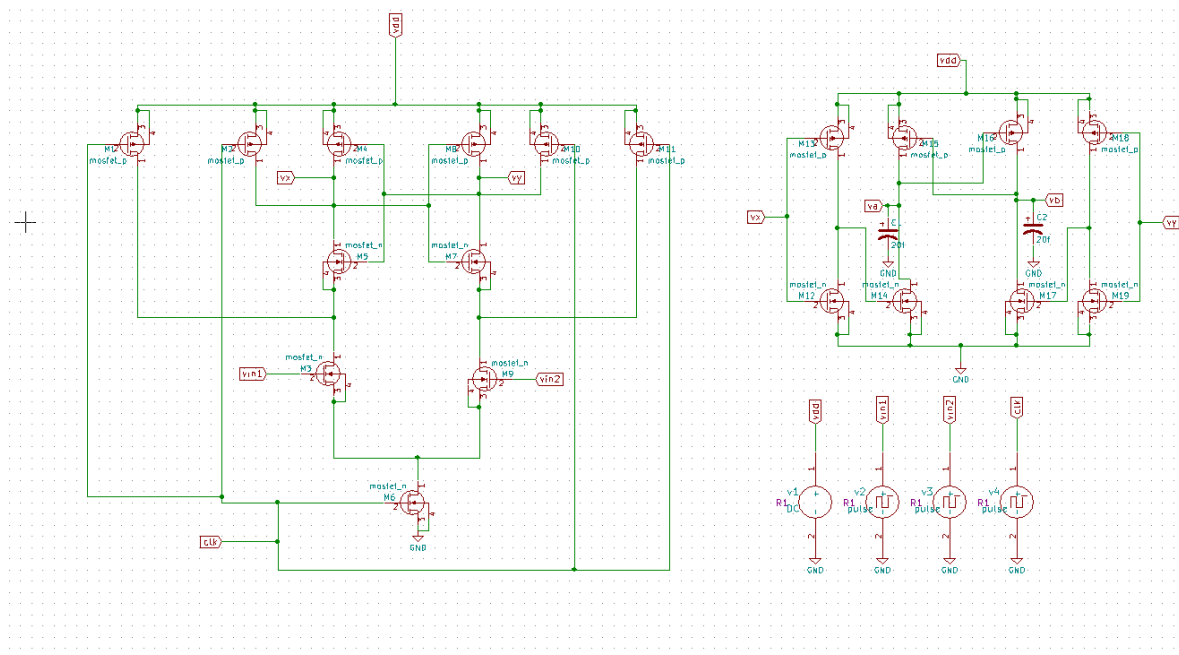
Department: Department of electronics engineering

College: Madras Institute of Technology, Anna University, Chennai

Introduction:

A differential Comparator is an integral part of analog to digital converters where it is used to perform quantisation and sampling. A standard opamp as a comparator is not preferred for these applications as it reduces the maximum sampling frequency that could be attained. In this design, a strongArm latch is used as the comparator core and is chosen as the core for this circuit because it consumes zero static power, produces full swing rail to rail outputs, requires single clock phase and provides higher sampling bandwidth. The strongArm latch stage is followed by a RS latch which is used to hold the output data during precharge phase of the strongArm latch.

Circuit Diagram:



Values of Input Sources:

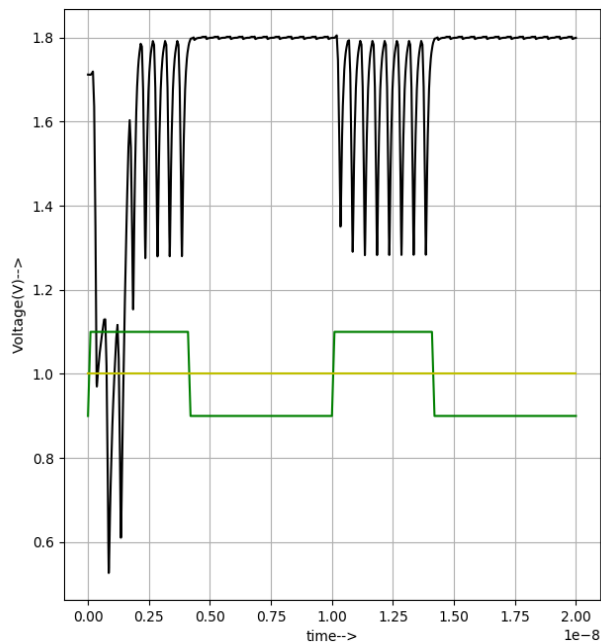
Add parameters for DC source v1	
Enter value (Volts/Amps):	1.8

Add parameters for pulse source v4	
Enter initial value (Volts/Amps):	0
Enter pulsed value (Volts/Amps):	1.8
Enter delay time (seconds):	0
Enter rise time (seconds):	0.05n
Enter fall time (seconds):	0.05n
Enter pulse width (seconds):	0.25n
Enter period (seconds):	0.5n

Add parameters for pulse source v3	
Enter initial value (Volts/Amps):	1
Enter pulsed value (Volts/Amps):	1
Enter delay time (seconds):	0
Enter rise time (seconds):	1p
Enter fall time (seconds):	1p
Enter pulse width (seconds):	1u
Enter period (seconds):	2u

Add parameters for pulse source v2	
Enter initial value (Volts/Amps):	0.9
Enter pulsed value (Volts/Amps):	1.1
Enter delay time (seconds):	0
Enter rise time (seconds):	0.1n
Enter fall time (seconds):	0.1n
Enter pulse width (seconds):	4n
Enter period (seconds):	10n

Simulated Output:

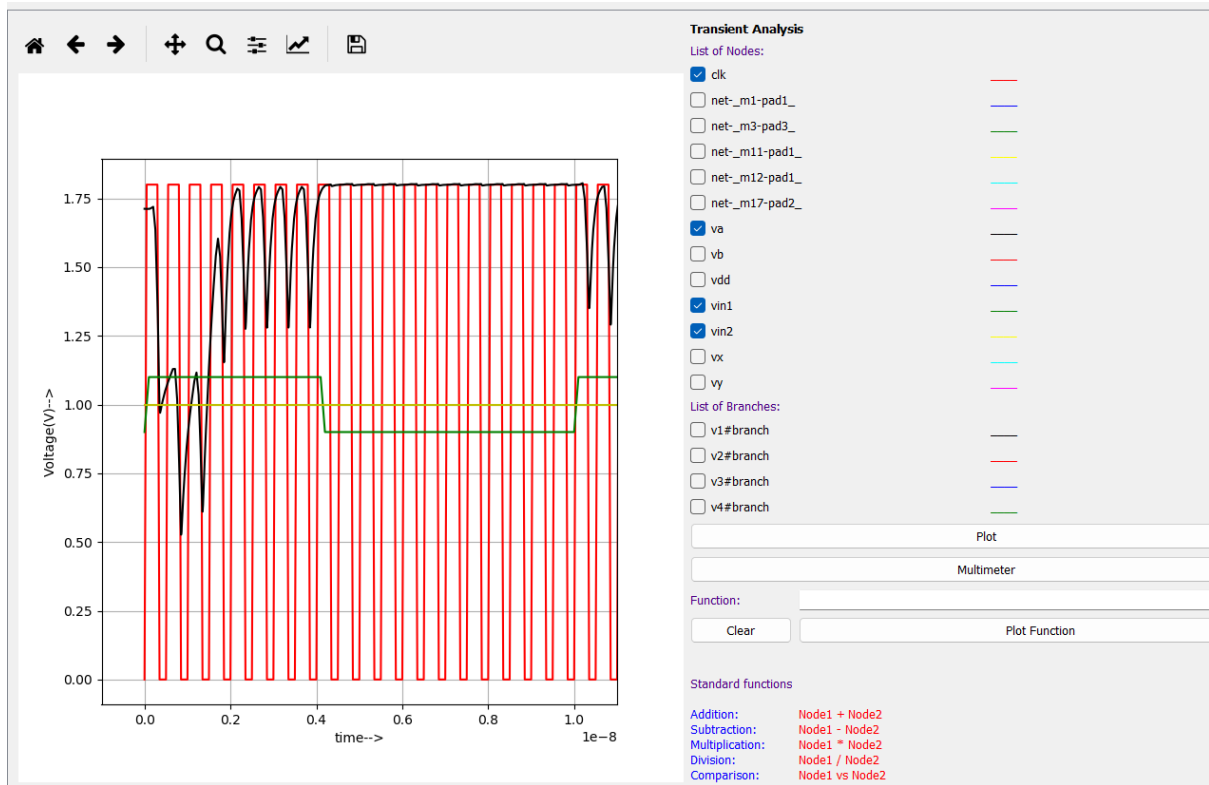


List of Branches:	
<input type="checkbox"/> net_m10-pad2_	
<input type="checkbox"/> net_m11-pad1_	
<input type="checkbox"/> net_m12-pad1_	
<input type="checkbox"/> net_m17-pad2_	
<input checked="" type="checkbox"/> va	
<input type="checkbox"/> vb	
<input type="checkbox"/> vdd	
<input checked="" type="checkbox"/> vin1	
<input checked="" type="checkbox"/> vin2	
<input type="checkbox"/> vx	
<input type="checkbox"/> vy	
<input type="checkbox"/> v1#branch	
<input type="checkbox"/> v2#branch	
<input type="checkbox"/> v3#branch	
<input type="checkbox"/> v4#branch	

Plot	
Multimeter	

Function:	
Clear	Plot Function

Standard functions	
Addition:	Node1 + Node2
Subtraction:	Node1 - Node2
Multiplication:	Node1 * Node2
Division:	Node1 / Node2



Inference:

In a dynamic latched comparator, two distinct phases govern its operation: the reset phase and the evaluation phase. The reset phase initiates when the clk signal transitions low, causing the output va go high as it gets charged to Vdd. During this phase, the comparator is prepared for the upcoming comparison. The actual comparison of the inputs takes place in the evaluation phase, which commences when the CLK signal transitions high. In this phase, the output Va goes high when $V_{in2} > V_{in1}$, indicating that the positive input voltage is greater than the negative input voltage. Conversely, the output Va goes high when $V_{in2} < V_{in1}$, signifying that the positive input voltage is less than the negative input voltage.

Reference:

<https://github.com/satishkumarl2002/StrongARM-Latch-based-Analog-Comparator>

P. Kishore, V. Tarun, S. R. V. S. Siva, and S. Kompella, "Design of Strong-Arm Latch Comparator for Low Power 12-bit SAR ADC," in *Proc. 2024 Int. Conf. Integr. Circuits Commun. Syst. (ICICACS)*, 2024.