

# Full Subtractor Circuit Design and Simulation

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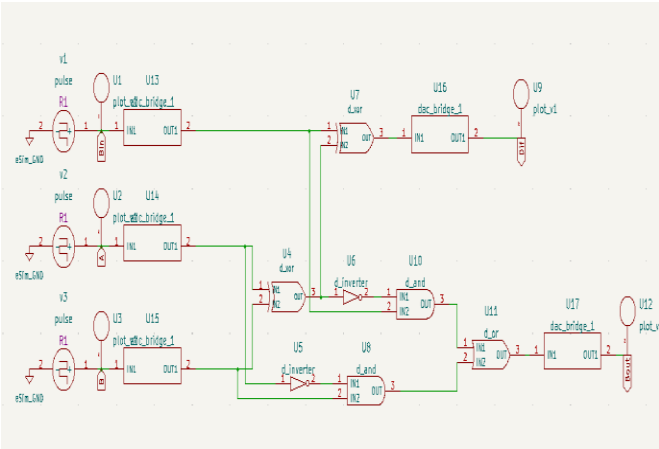
**Abstract**—This project presents the design and verification of a 1-bit Full Subtractor using fundamental logic gates, which ensures optimized performance in terms of area, power, and speed. The design exploits the Boolean properties of difference and borrow generation to realize efficient gate-level implementation with minimal transistor usage. By combining XOR, AND, and NOT gates, the circuit achieves accurate subtraction with a compact structure, reducing redundancy and improving switching efficiency. The circuit was modeled and simulated using eSim, an open-source EDA tool, and its functional correctness was verified through Ngspice transient analysis. The simulation results confirm accurate outputs for all binary input combinations, validating the suitability of logic gate design for compact and power-efficient arithmetic units in VLSI systems.

**Index Terms**—Logic gates, Boolean algebra, Transistor minimization, Low power

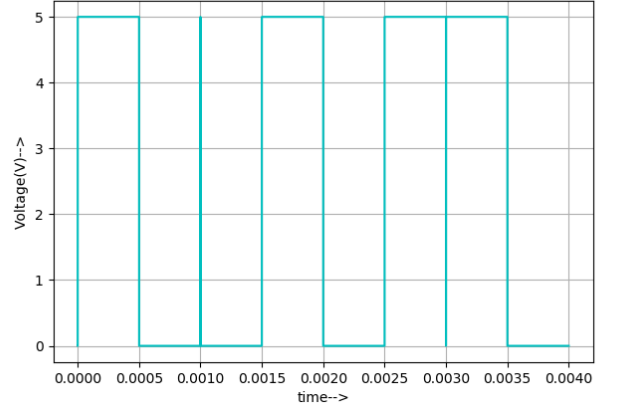
## I. INTRODUCTION

In modern digital systems, arithmetic logic units (ALUs) play a pivotal role in performing computational tasks, and the full subtractor is an essential component within these units. With the growing demand for compact, high-speed, and low-power integrated circuits, designing efficient full subtractors has become a significant focus area in VLSI research. Conventional CMOS logic styles, though functionally reliable, often employ redundant transistors that increase power consumption and area. Logic gate-based design emerges as a promising alternative due to its simplicity and minimized transistor count. This approach leverages Boolean properties to implement difference and borrow operations in a structurally efficient manner. Such designs not only simplify hardware realization but also improve performance by reducing delay paths and lowering parasitic effects.

## II. IMPLEMENTATION



## III. RESULT



The waveform illustrates the Difference output of the 1-bit full subtractor implemented using logic gates. Simulated in eSim with Ngspice, the output correctly transitions between logic levels (0 V and 5 V) for all eight input combinations of A, B, and Bin. The consistent and accurate transitions validate the correct functionality of the subtractor. Minor overshoots are observed due to switching dynamics but do not affect logic integrity. Overall, the Difference output confirms the successful implementation of gate-level logic for subtraction operations.

## IV. CONCLUSION

This research presented the design and analysis of a 1-bit full subtractor using logic gates. The proposed design achieved minimal transistor usage with accurate outputs across all input states, confirming its efficiency for compact and low-power VLSI arithmetic units.

## V. REFERENCES

S. Suma and V. Kiran, *Design and Analysis of a Full Subtractor using Various Design Techniques*, n.d.