

Research Migration Project

National Institute of Technology Rourkela

Name of the participant : Krishnendu Roy

Title of the circuit : 2:1 Multiplexer Using Different Design Styles: Comparative Analysis

Abstract:

Multiplexers (MUX) are essential components in digital circuits, enabling efficient data selection and signal routing. This project focuses on the design and comparative analysis of a 2:1 multiplexer using different design styles, including conventional CMOS, Transmission Gate Logic (TGL), and Pass Transistor Logic (PTL). Simulations are performed to analyze trade-offs between power efficiency and switching speed, providing insights into the advantages and limitations of each design style. The results demonstrate how different approaches impact circuit performance, making them suitable for various applications in low-power and high-speed digital systems. By comparing these methodologies, this study serves as a valuable reference for researchers and engineers working on optimized multiplexer designs in modern VLSI circuits.

Theory/Description :

A **2:1 multiplexer (MUX)** is a combinational circuit that selects one of two input signals (I_0 or I_1) based on a select line (S) and routes it to the output (Y). The Boolean expression for its operation is:

$$Y = \overline{S} \cdot I_0 + S \cdot I_1$$

1. Transmission Gate (TG) Logic

Transmission gate logic uses both NMOS and PMOS transistors connected in parallel to form a bidirectional switch. This configuration allows for full-swing output voltage with minimal

voltage drop, ensuring strong logic levels. TG-based MUXes benefit from low on-resistance, leading to faster switching speeds. However, they require complementary control signals (S and $S^{\bar{}}$), which increases circuit complexity slightly. TG logic is particularly advantageous in high-speed and low-power applications where signal integrity is critical.

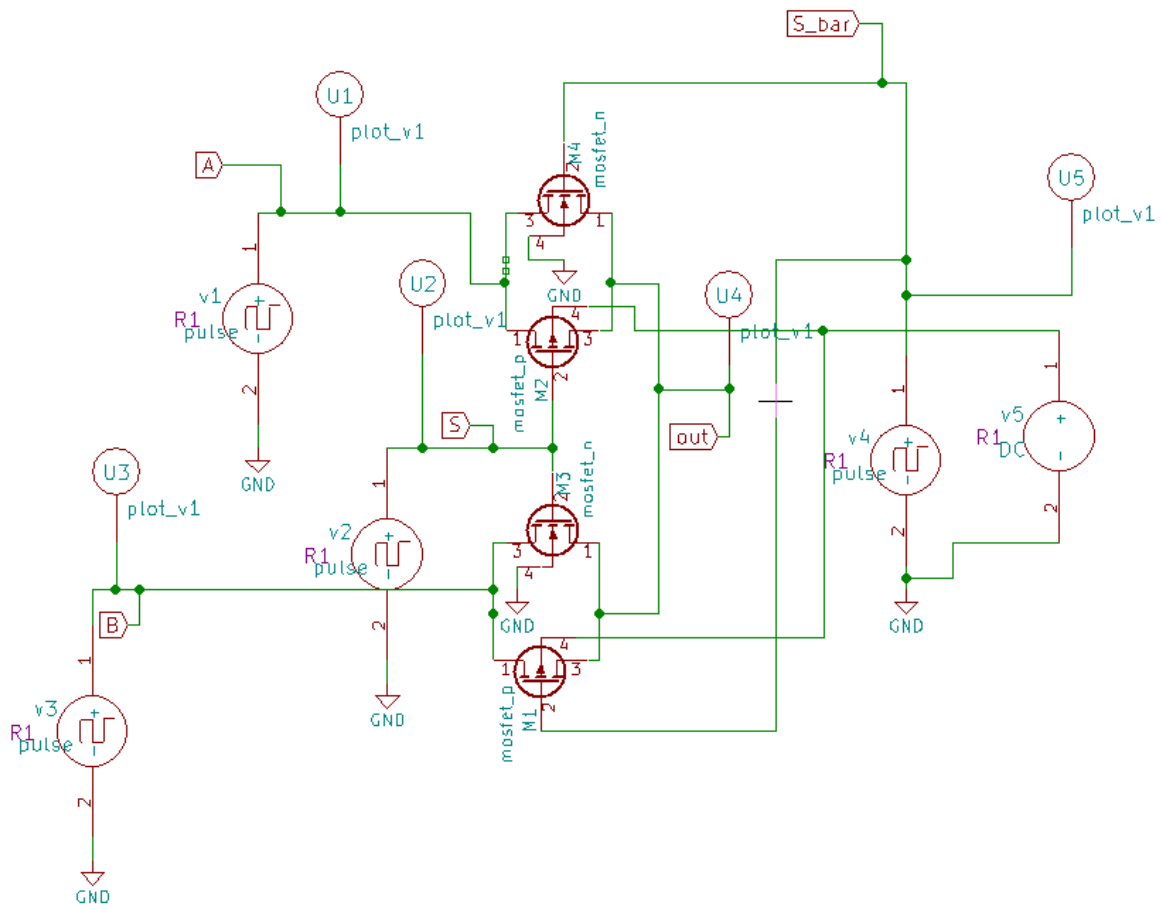
2. Pass Transistor Logic (PTL)

Pass transistor logic relies on either NMOS or PMOS transistors alone to pass signals from input to output. While PTL reduces transistor count, it suffers from threshold voltage loss, especially when transmitting a logic '1' through an NMOS transistor. This results in degraded output levels, requiring additional level restoration circuits in some cases. Despite this drawback, PTL offers significant area savings and lower power consumption compared to CMOS, making it useful in compact and energy-efficient designs.

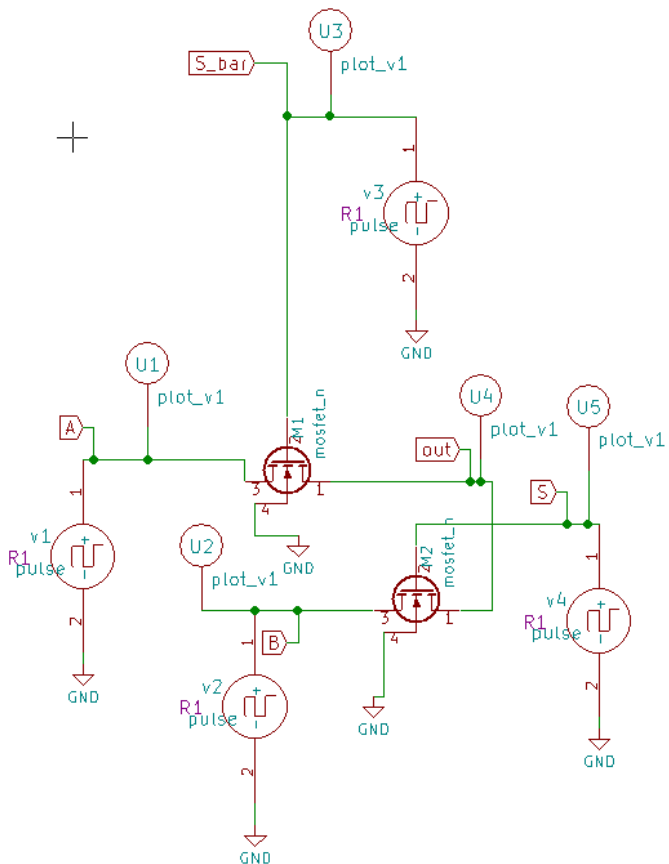
3. CMOS Logic

CMOS logic implements the MUX using complementary pull-up (PMOS) and pull-down (NMOS) networks, ensuring robust operation with full voltage swing and high noise margins. Unlike PTL and TG, CMOS does not suffer from signal degradation, making it highly reliable. However, this comes at the cost of increased transistor count, leading to higher power consumption and larger chip area. CMOS-based MUXes are widely used in general-purpose digital circuits where stability and noise immunity are prioritized over area and power efficiency.

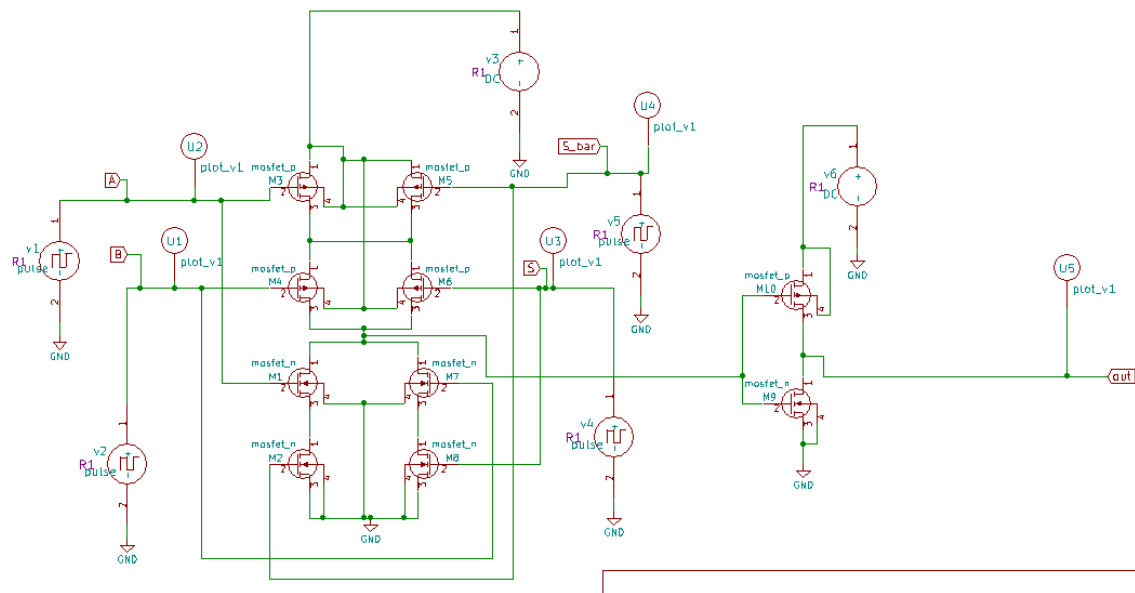
Circuit Diagram(s) :



2:1 MUX using transmission gate only



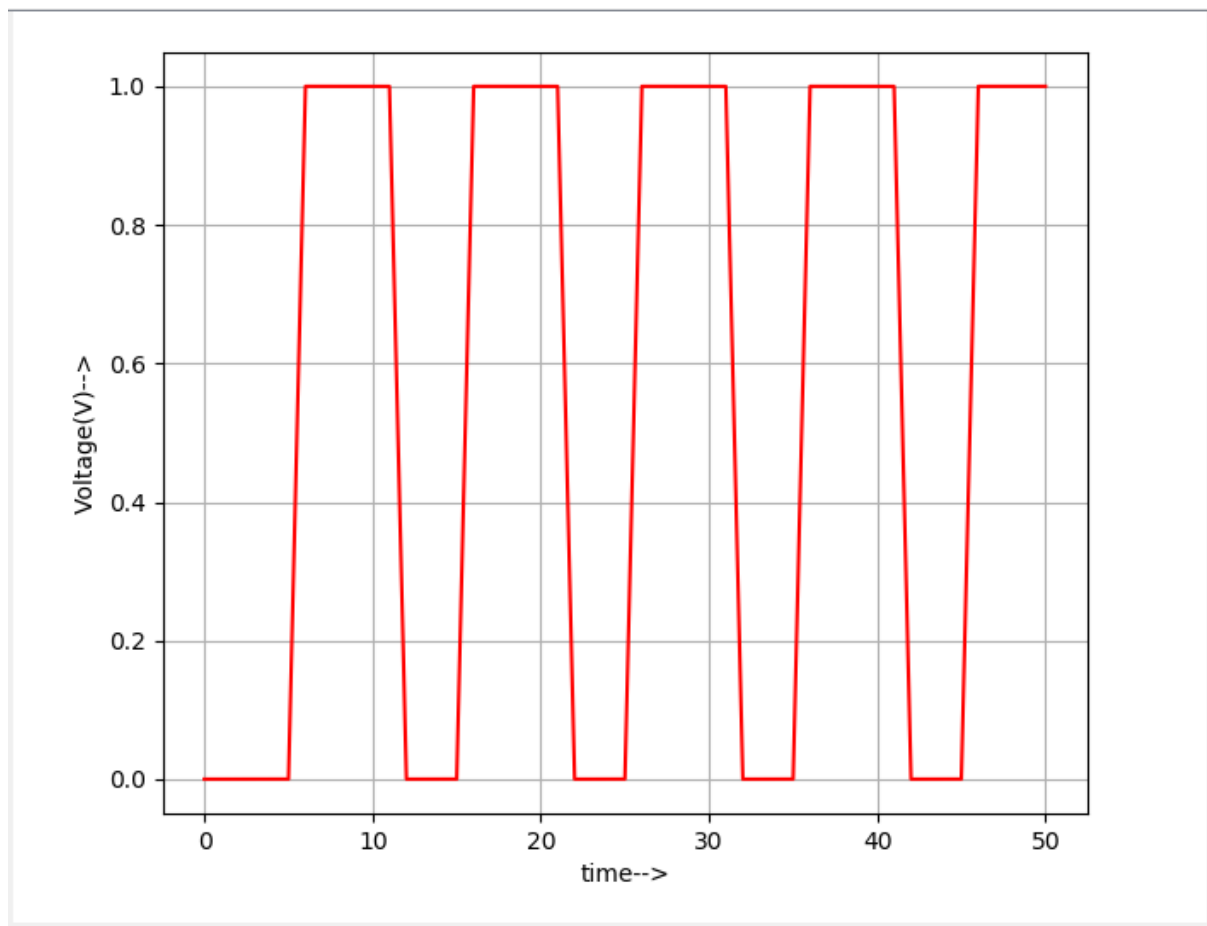
2:1 MUX using pass transistor only



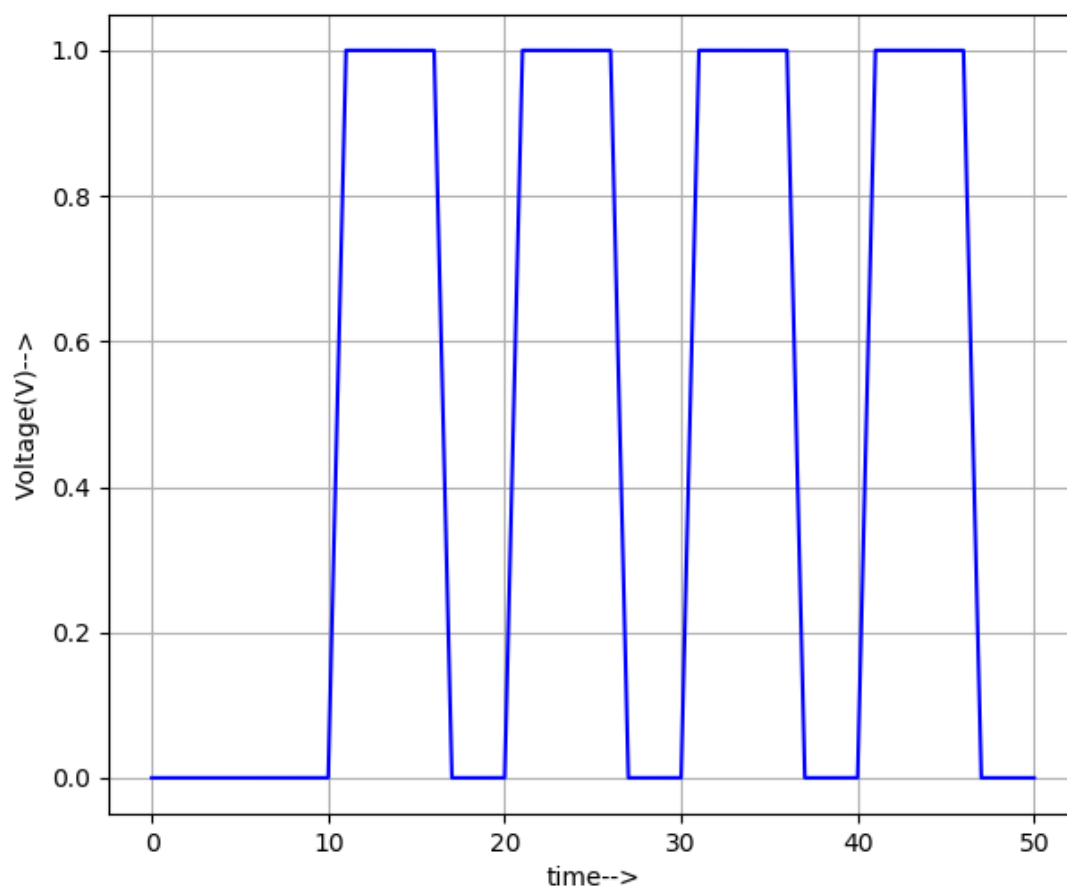
2:1 MUX using CMOS logic only

Results (Input, Output waveforms and/or Multimeter readings) :

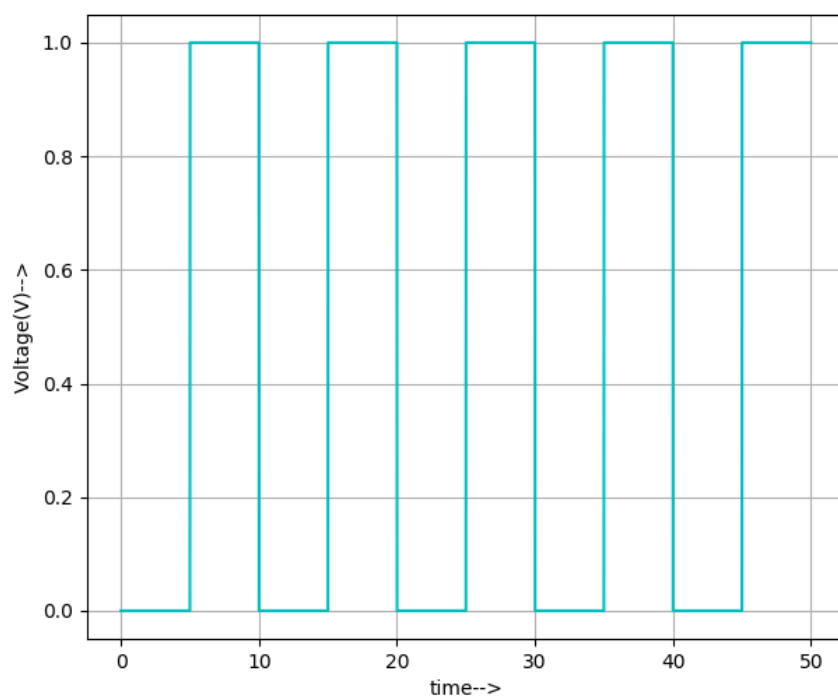
For a:



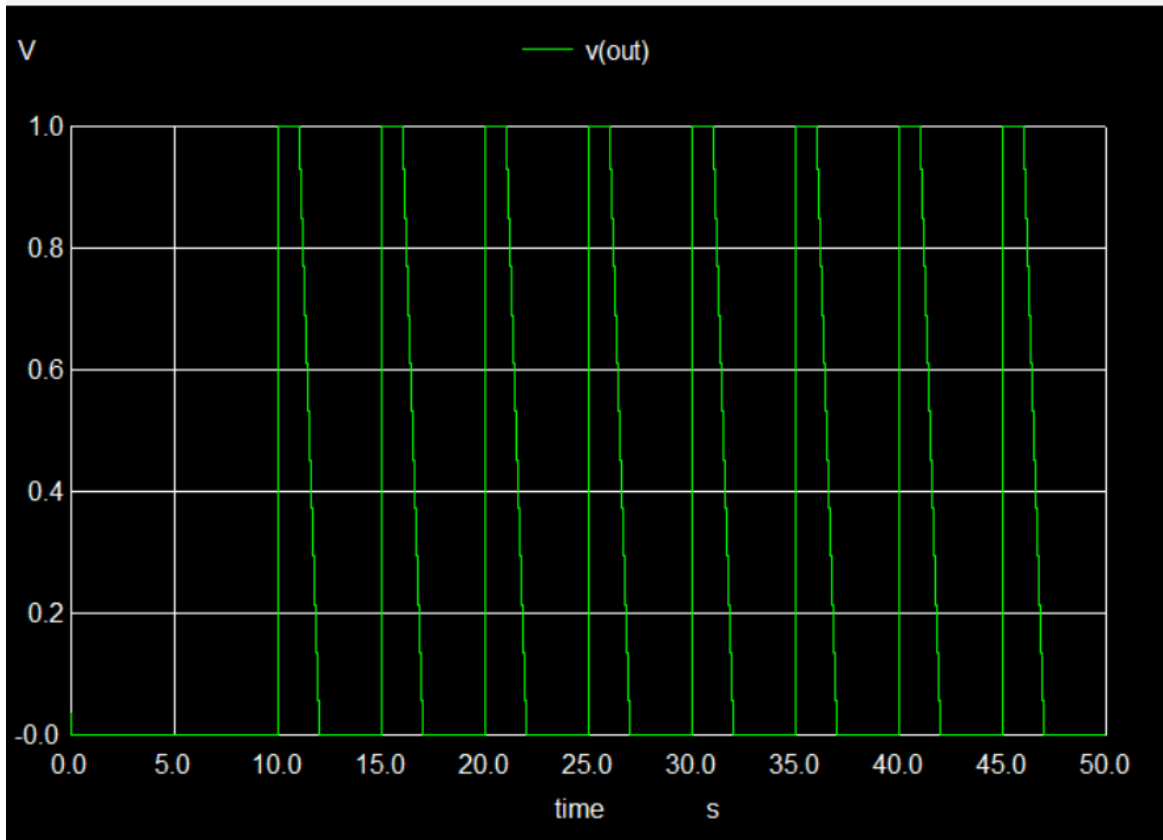
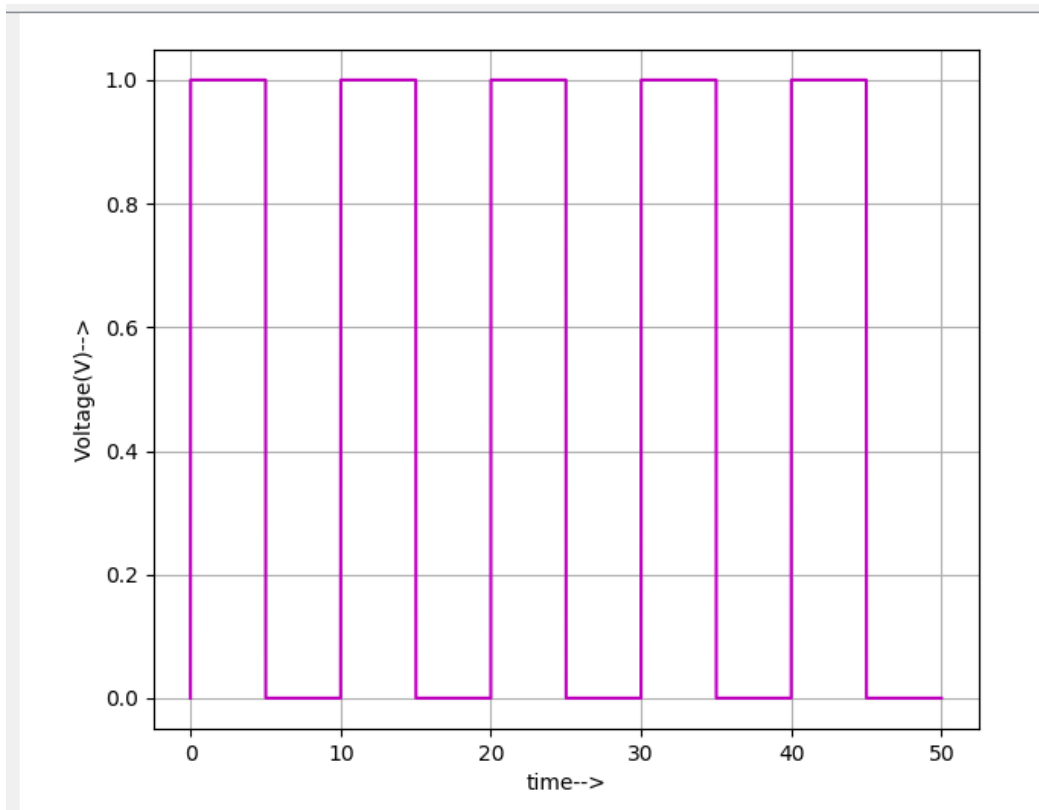
For b:



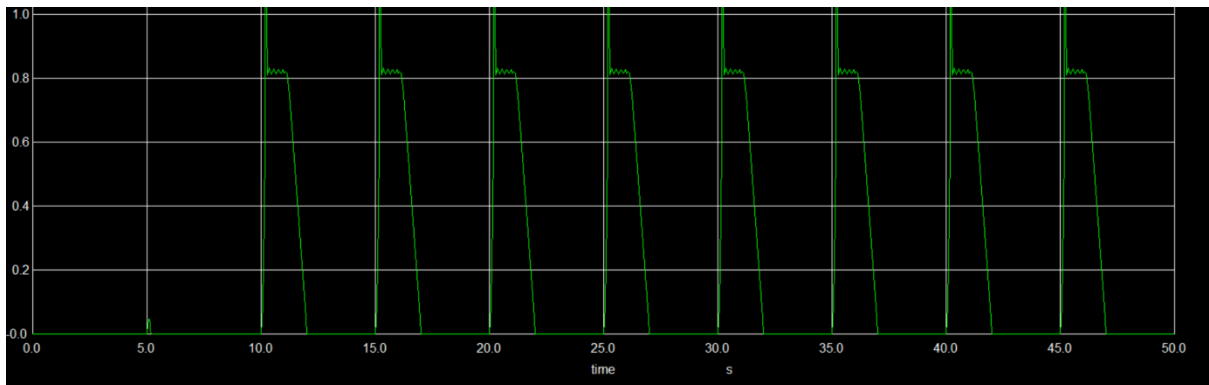
For s:



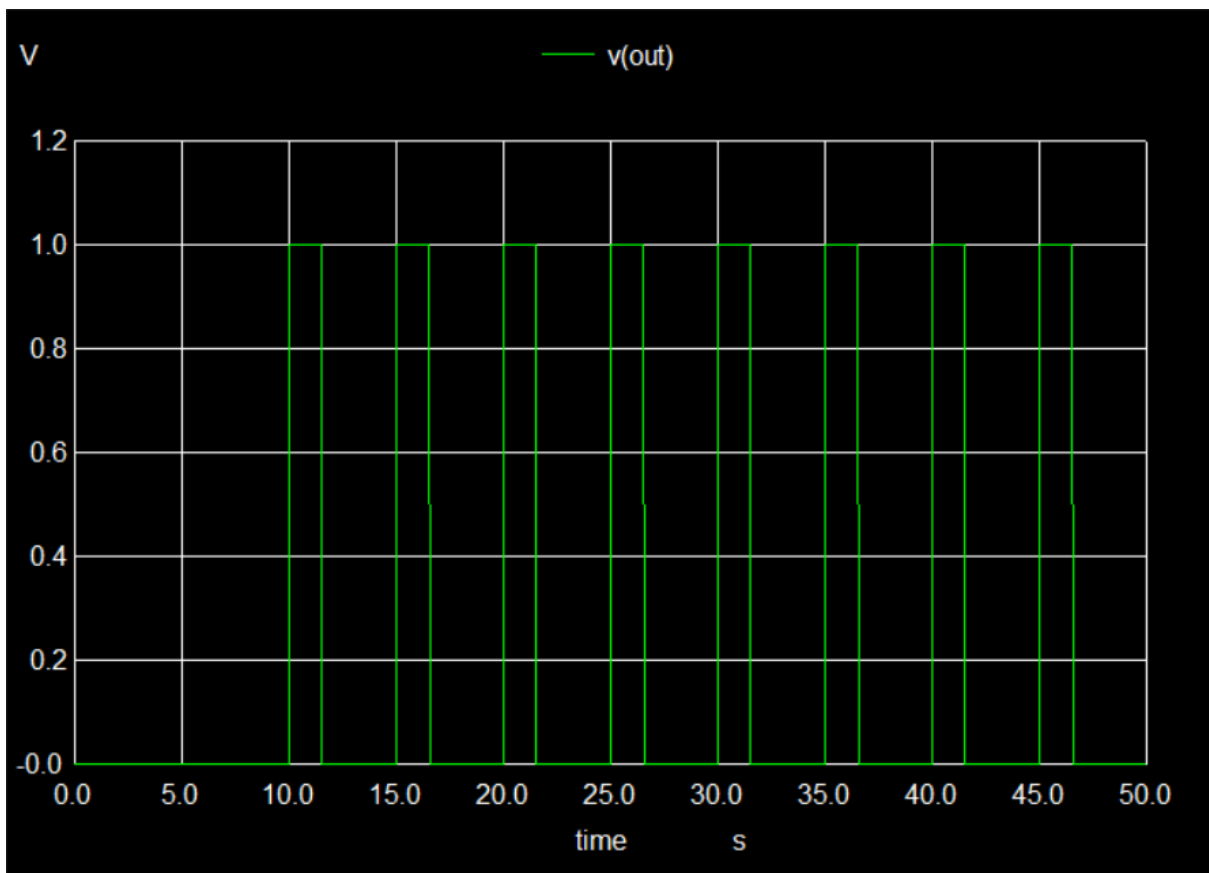
For S_{bar} :



Simulation waveform of 2:1 MUX using transmission gate only.



Simulation waveform of 2:1 MUX using pass transistors only



Simulation waveform of 2:1 MUX using CMOS logic

Conclusion :

This study compared three 2:1 MUX designs—**TG, PTL, and CMOS logic**—revealing key trade-offs. **TG logic** offers high speed and signal integrity but needs complementary signals. **PTL** minimizes area and power but suffers from voltage degradation. **CMOS** ensures robustness at the cost of higher power and area. The optimal choice depends on application priorities—speed (TG), efficiency (PTL), or reliability (CMOS).

Source/Reference(s) :

Title of Paper: 2:1 Multiplexer Using Different Design Styles: Comparative Analysis

Link to paper: [\(PDF\) 2:1 Multiplexer Using Different Design Styles: Comparative Analysis](#)