

TR gate Based Design of Reversible Full Subtractor Using CMOS

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Abstract

The reversible full subtractor, a crucial component in low-power VLSI design, addresses the increasing demand for energy-efficient computing. With applications in quantum computing, cryptography, and nanotechnology, reversible logic has become a key research area in modern technology. This paper presents the design, implementation, and verification of a reversible full subtractor using CMOS technology, utilizing eSim for simulation and analysis. The implementation is evaluated based on power dissipation, propagation delay, and transistor count to ensure optimized performance. eSim and NgSpice simulation results validate the accuracy and efficiency of the proposed design, confirming its feasibility for low-power VLSI applications. This study provides an in-depth exploration of the reversible full subtractor's architecture, its significance in contemporary digital systems, and its potential to enhance the development of energy-efficient computing technologies.

Keywords: Reversible full subtractor, novel reversible gate, TR gate, eSim software, NgSpice simulation

1. Introduction

TR Gate (Toffoli Reversible Gate) is a universal reversible gate, meaning any reversible logic function can be constructed using TR gates. **Full Subtractors** are fundamental building blocks in arithmetic circuits, responsible for subtracting one binary digit from another, considering a borrow from a previous stage. Reversible full subtractor is formed using two TR gates that reduces a part of the quantum cost than the conventional full subtractor circuit. The inputs of the gate are A, B, 0 and the outputs are Q ($Q = C$), Borrow ($C \oplus (A \oplus B)' \oplus A'B$) and the difference ($A \oplus B \oplus C$).

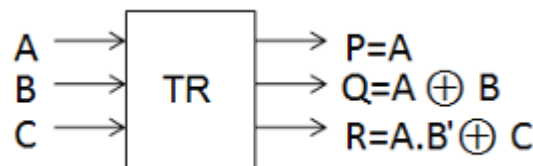


Figure 1.a. Block diagram of TR Gate

2. Purpose of Reversible full subtractor

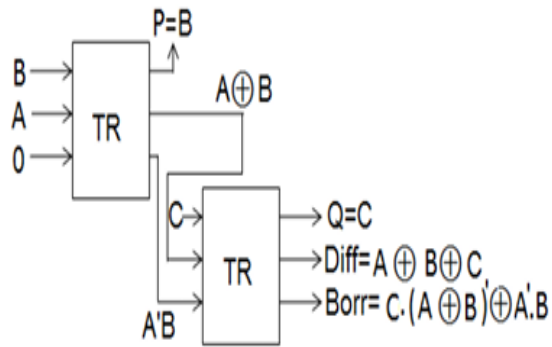
Reversible full subtractor is used in various applications due to its unique characteristics. It is known for its

Preserving Information: Unlike conventional subtractors, reversible subtractors prevent data loss, which helps reduce power dissipation.

Minimizing Power Consumption: Since energy dissipation is directly related to information loss, reversible logic helps achieve low-power computing, making it ideal for quantum computing and low-power VLSI applications.

Quantum Computing Applications: Reversible logic is essential for quantum circuits, where information loss is not allowed. The TR gate-based subtractor can be used in quantum arithmetic operations.

3. Proposed Circuit



A	B	C		Borr	Diff
0	0	0		0	0
0	0	1		1	1
0	1	0		1	1
0	1	1		1	0
1	0	0		0	1
1	0	1		0	0
1	1	0		0	0
1	1	1		1	1

Figure 3.a. Block diagram of TR based Reversible Full Subtractor,
3.b. Truth Table of Full Subtractor

Figure 3.a. shows the block diagram of the TR based Reversible Full Subtractor with three inputs and its corresponding three outputs with special logic functions. The output of the circuit with respect to the input can be easily retrieved and verified using its truth table shown in Figure 3.b.

4. Schematic Diagram

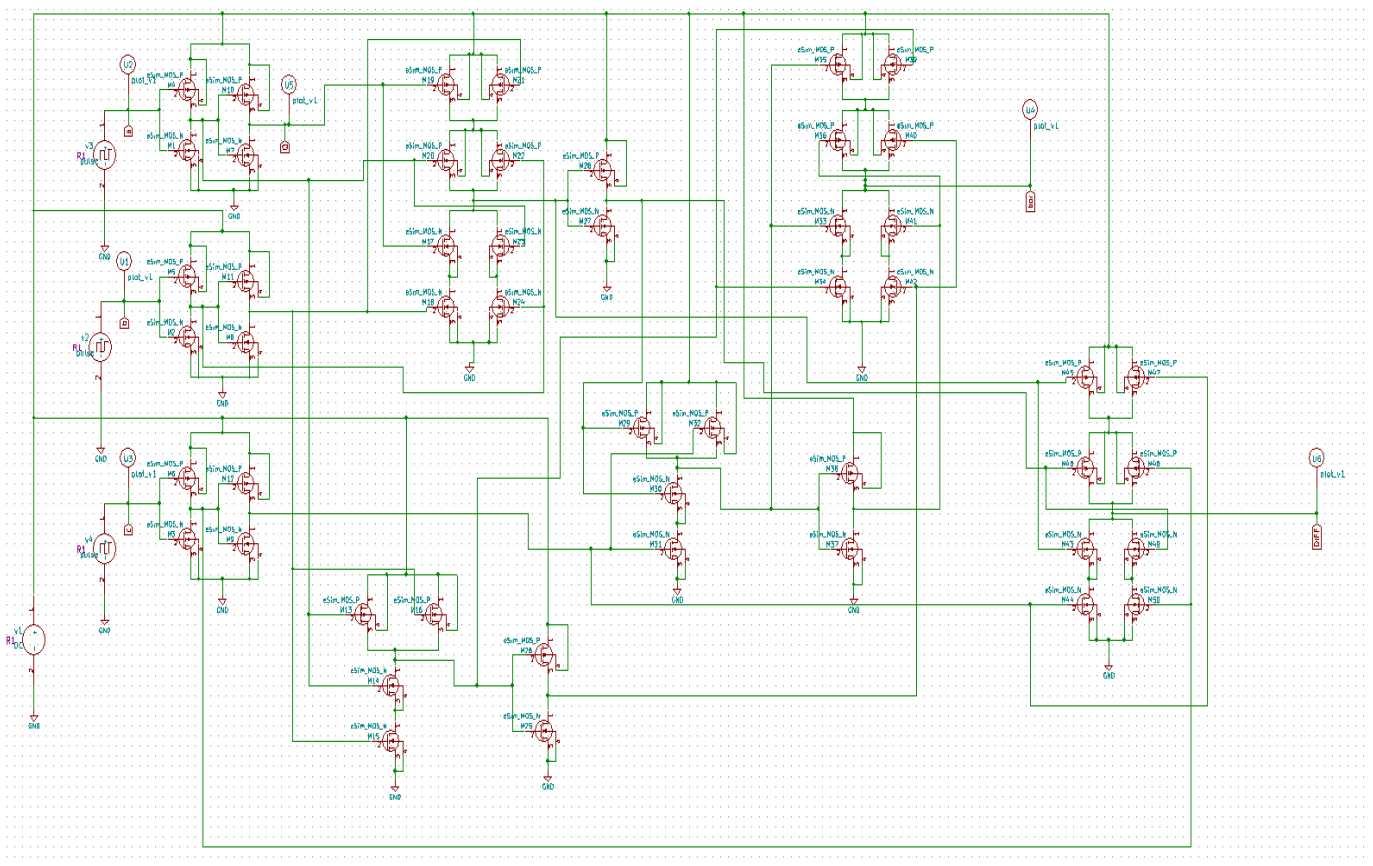
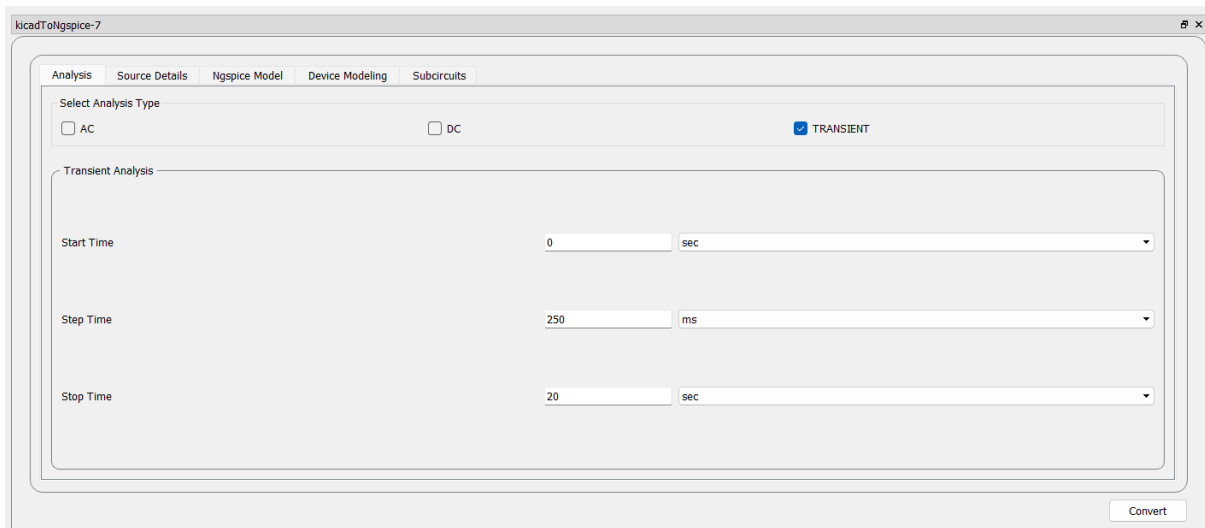


Fig 4.a. Schematic diagram of TR based Reversible Full Subtractor using CMOS

5. NgSpice Simulation

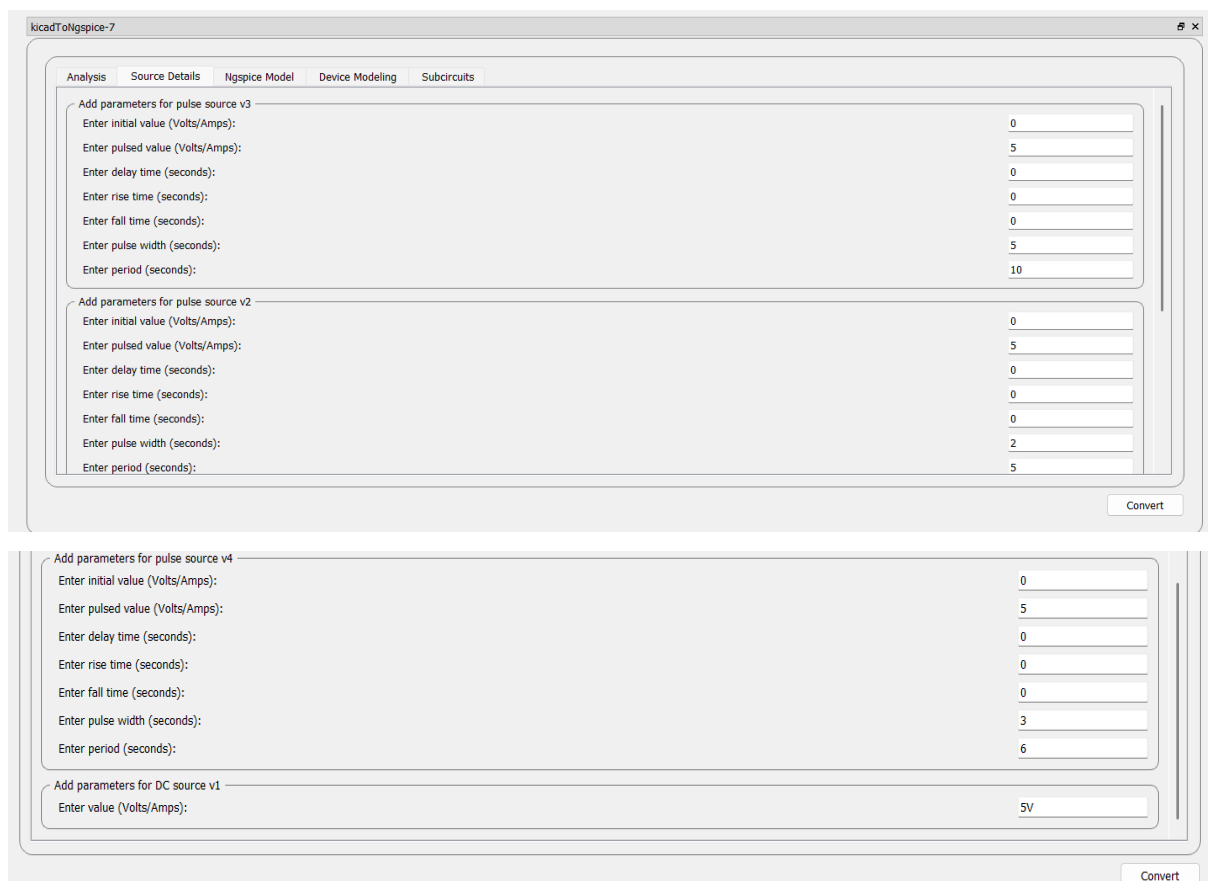
5.a. Transient Analysis:



The screenshot shows the 'kicadToNgspice-7' window with the 'Analysis' tab selected. Under 'Select Analysis Type', the 'TRANSIENT' checkbox is checked. The 'Transient Analysis' section contains three input fields: 'Start Time' set to 0 sec, 'Step Time' set to 250 ms, and 'Stop Time' set to 20 sec. A 'Convert' button is located at the bottom right.

Figure 5.a. Transient Analysis of Reversible Full Subtractor

5.b. Source Details:



The screenshot shows the 'kicadToNgspice-7' window with the 'Source Details' tab selected. It displays configuration for three pulse sources (v3, v2, v4) and one DC source (v1). Each pulse source has fields for initial value, pulsed value, delay time, rise time, fall time, pulse width, and period. The DC source has a field for its value. A 'Convert' button is at the bottom right.

Source	Initial Value (Volts/Amps)	Pulsed Value (Volts/Amps)	Delay Time (seconds)	Rise Time (seconds)	Fall Time (seconds)	Pulse Width (seconds)	Period (seconds)
v3	0	5	0	0	0	5	10
v2	0	5	0	0	0	2	5
v4	0	5	0	0	0	3	6
v1 (DC)	5V						

Figure 5.b. Source details of one biasing voltage and three input pulses with different clock pulses.

5.c Device Modeling:

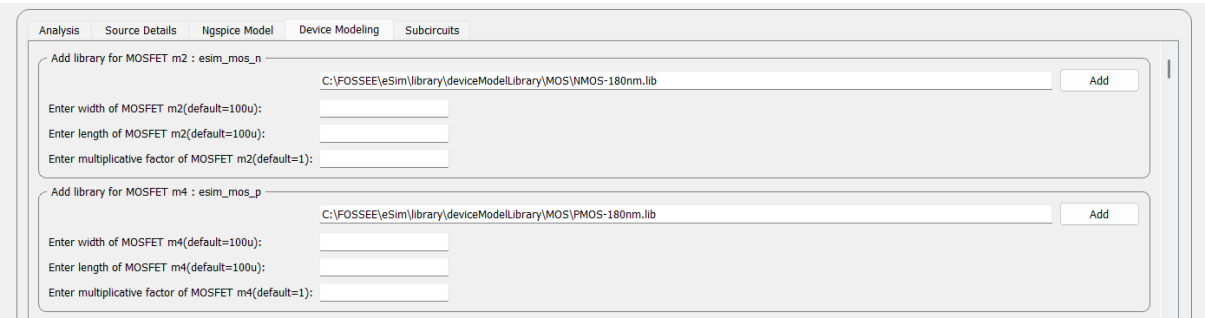
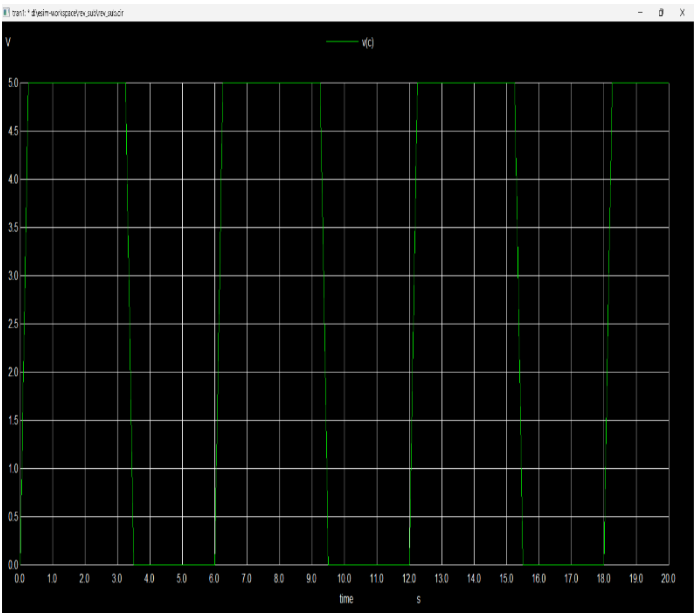


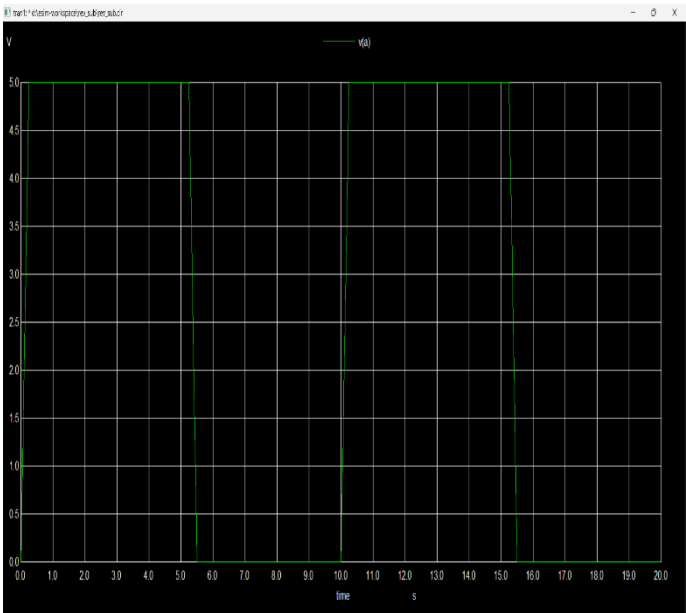
Figure 5.c. Device Modeling of PMOS and CMOS circuits used here

The width and length of the eSim NMOS and PMOS are set to be default, and the library file is added with the NMOS and PMOS 180nm program files.

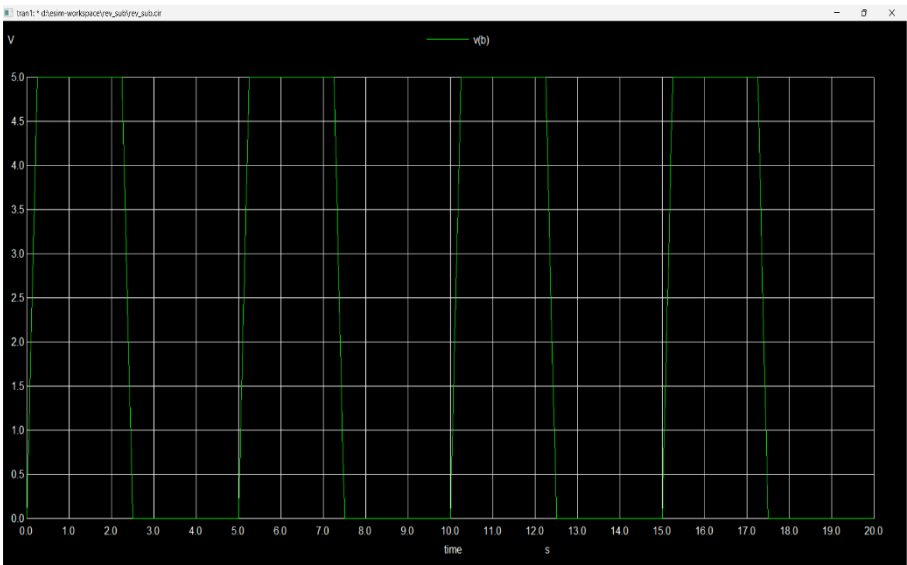
5.d. Input Waveforms:



(a)



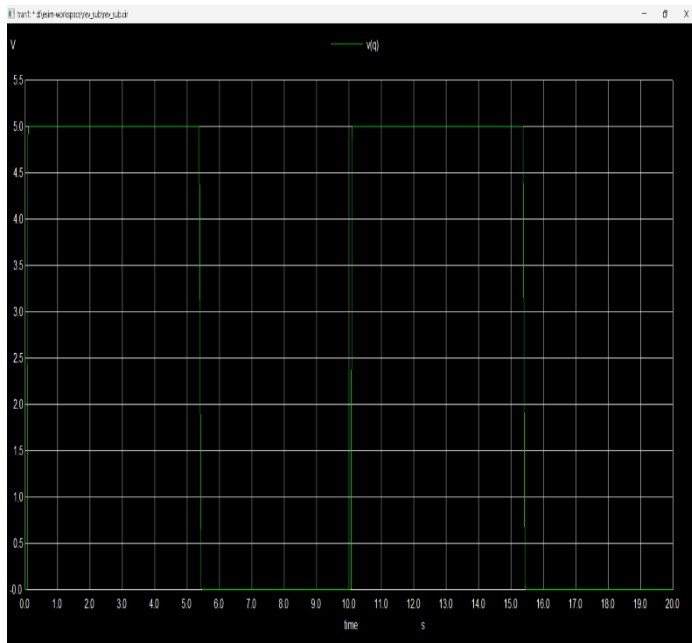
(b)



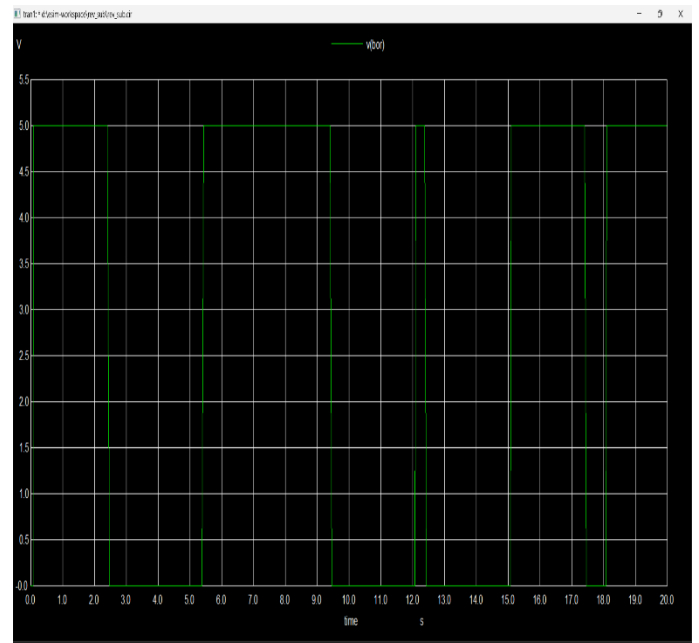
(c)

Figure 5.d. (a), (b), (c) Input waveforms for the input pulses

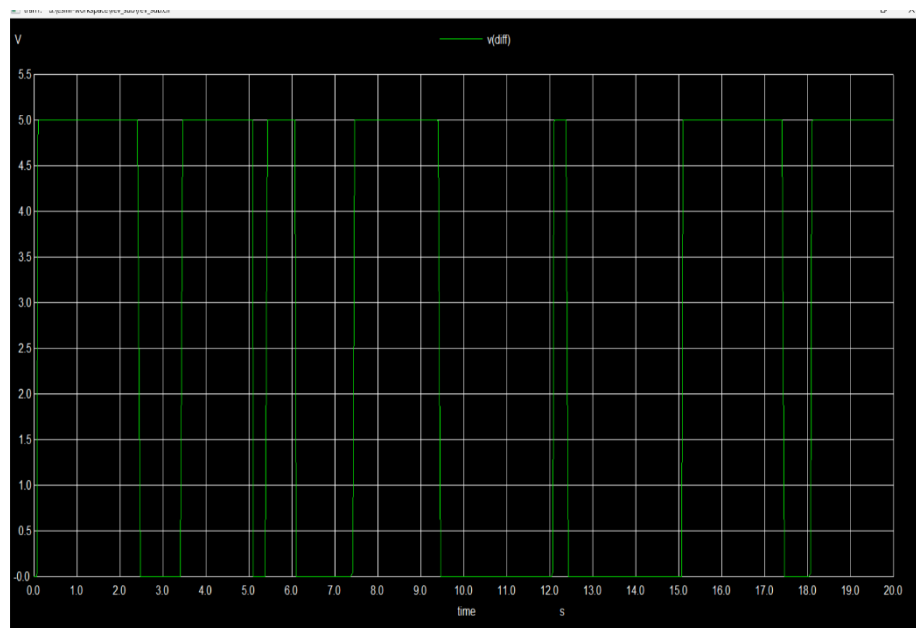
5.e. Output Waveforms



(a)



(b)

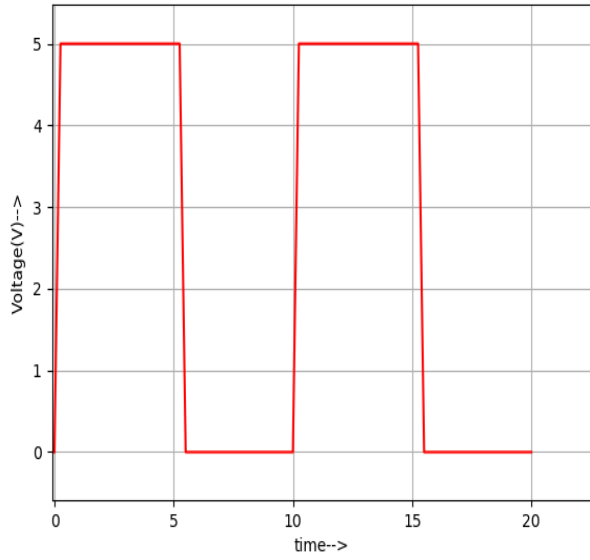


(c)

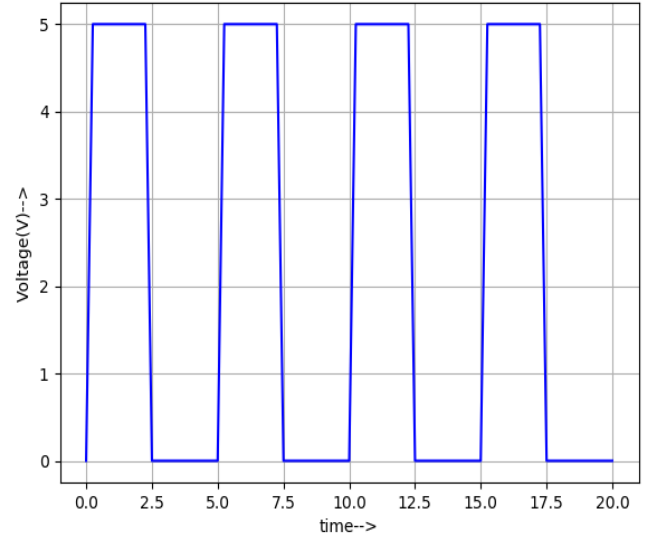
Figure 5.e. (a), (b), (c) 3 Output waveforms of the Reversible Full Subtractor in NgSpice simulation

6. Python Plot

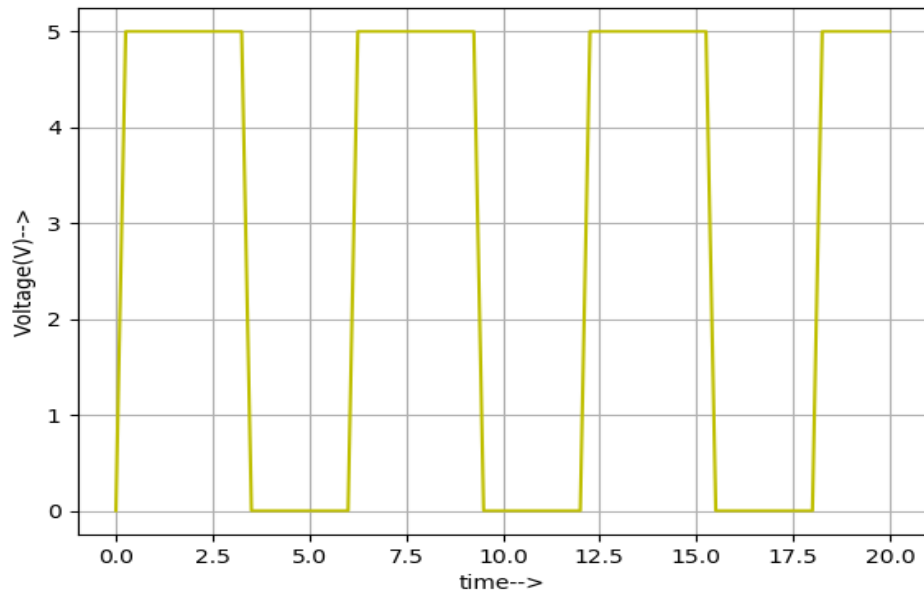
6.a. Input Waveforms



(a)



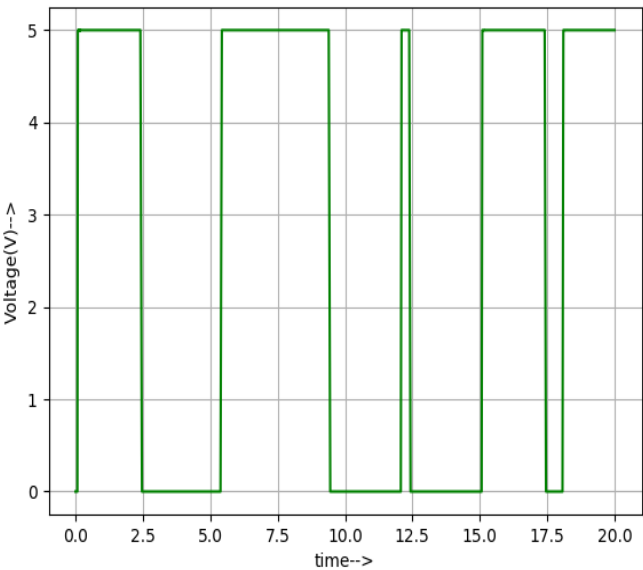
(b)



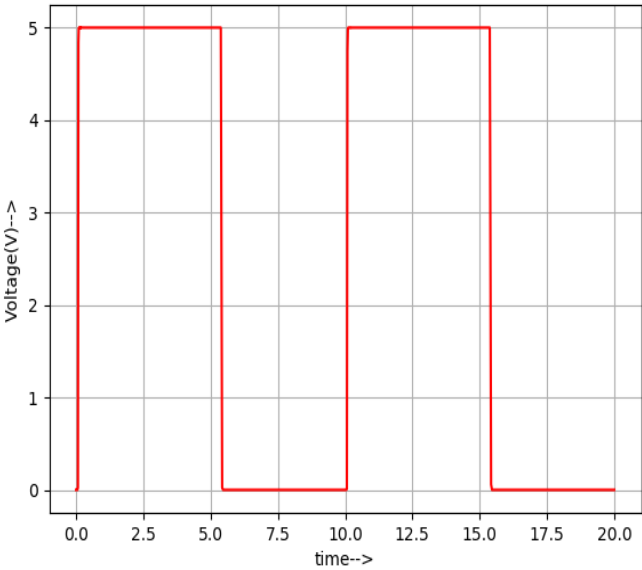
(c)

Figure 6.a (a), (b) Input Waveforms for the input pulses in Python MatPlot

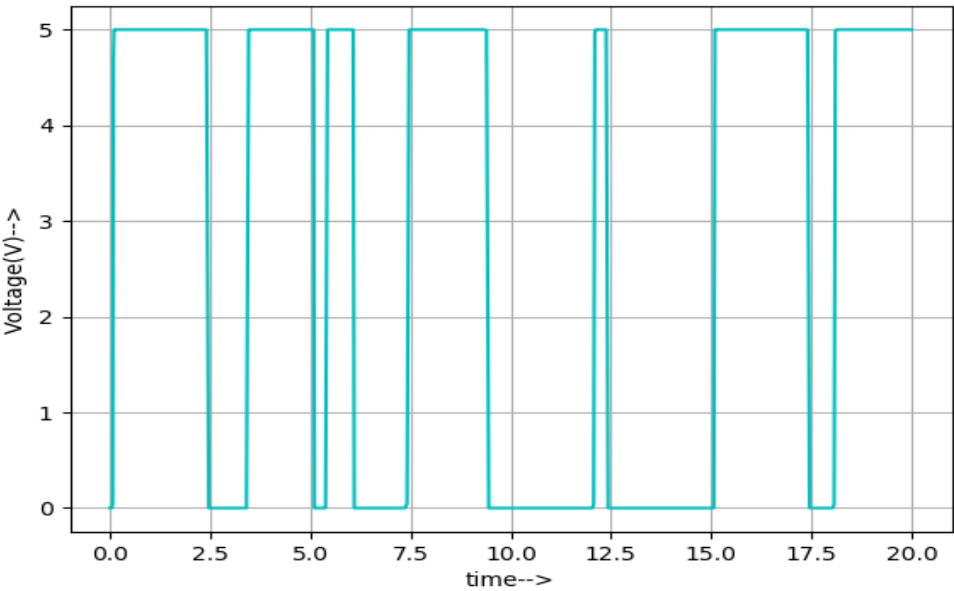
6.b. Output Waveforms



(a)



(b)



(c)

Figure 6.b. (a), (b), (c) 3 Output waveforms shows the results of the borrow, Q and the difference of the Reversible Full Subtractor respectively in Python MatPlot.

7. Conclusion

The TR based reversible full subtractor was successfully designed and simulated using CMOS technology in the eSim platform. The functionality was validated through NgSpice waveforms, and the outputs were further visualized and confirmed using Python's Matplotlib. The results aligned with the expected logical behaviour, demonstrating the accuracy and reliability of the full subtractor. This study establishes the full subtractor using the TR gate as a promising component for low-power and energy-efficient designs in modern VLSI systems, quantum computing showcasing its potential for practical applications in reversible logic circuits as well as reversible quantum logic circuits

8. References

Source :

1.TITLE : Design of Efficient Reversible Binary Subtractors Based on A New Reversible Gate

AUTHOR : Himanshu Thapliyal and Nagarajan Ranganathan

LINK :

https://ieeexplore.ieee.org/abstract/document/5076412?casa_token=Ge44z1H7nxcAAAAA:rU2p96NTJqQrF2wPA38Jzi9k-dvWzy826Oq9Iy_K5TT6RJvuNIEsOkWSCyc-PvHLc1hk5kQ6N4PW

2. TITLE : Design and Implementation of an Efficient Reversible Comparator Using TR Gate

AUTHOR : Subramanian Saravanan¹, Ila Vennila¹, Sudha Mohanram

LINK : <https://www.scirp.org/journal/paperinformation?paperid=69136>