LAHAF: Low-power, area-efficient, and high-performance approximate full adder based on static CMOS Implementation Using eSim

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Title of the circuit: LAHAF: Low-power, area-efficient, and high-performance approximate full adder based on static CMOS

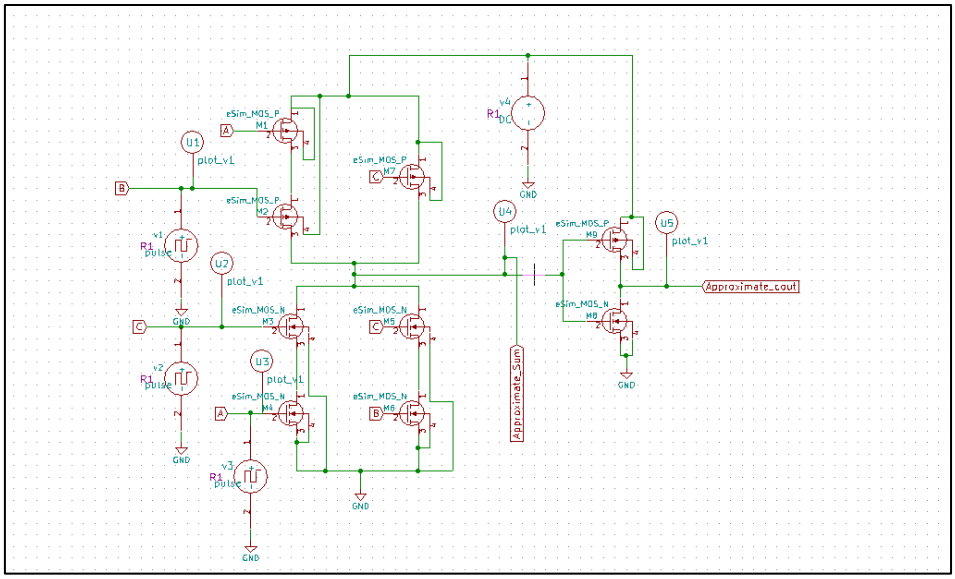
Description:

In this article, a low-power, area-efficient full adder cell is designed, and its approximate output is presented. Techniques such as Static CMOS, Pass Transistor Logic, Transmission Gate Logic, and similar structures are employed to achieve a low-power design approach. In this work, the Static CMOS structure is used to design an approximate low-power full adder, where the Sum output is inverted to generate the Carry.

Approximate adders are suitable for complex applications such as image processing, machine learning, and data mining. Due to the human visual system's tolerance to minor inaccuracies, approximate computing can effectively be applied in processing images and videos. These adders offer significantly low power dissipation, reduced area, and acceptable performance, making them ideal for power-constrained systems.

To achieve low power consumption, adopting an area-efficient design is a key strategy, as it also contributes to reducing overall fabrication cost. The proposed design is simulated using the eSim tool, and the overall propagation delay, average power consumption, and output waveforms are analyzed. The simulation results using Ngspice illustrate the input signals (A, B, and C) and the corresponding outputs of the approximate low-power full adder (Sum and Carry).

Circuit Diagram:



Truth Table:

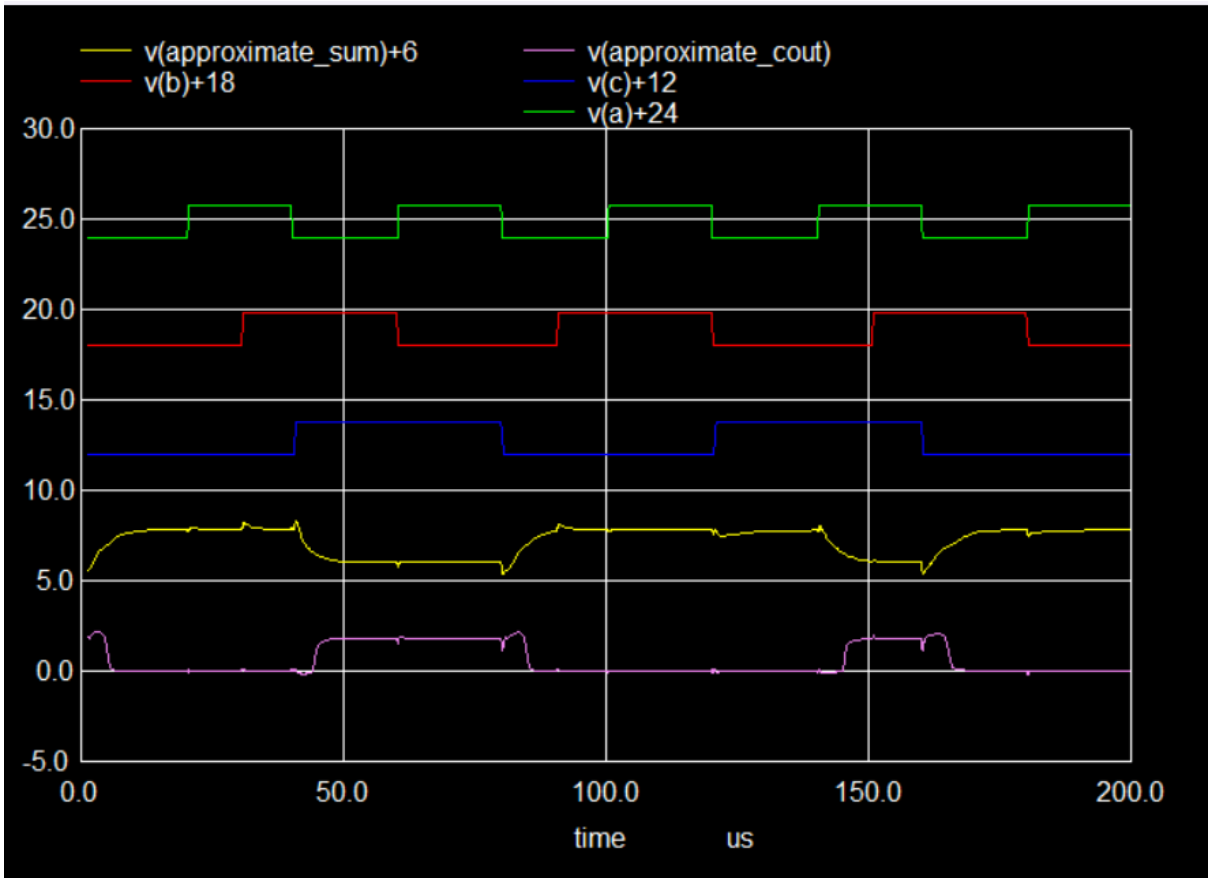
Table 1: truth table is adapted from Table 6 of the LAHAF journal [1].

The truth table of the exact full adder and the proposed approximate full adder.

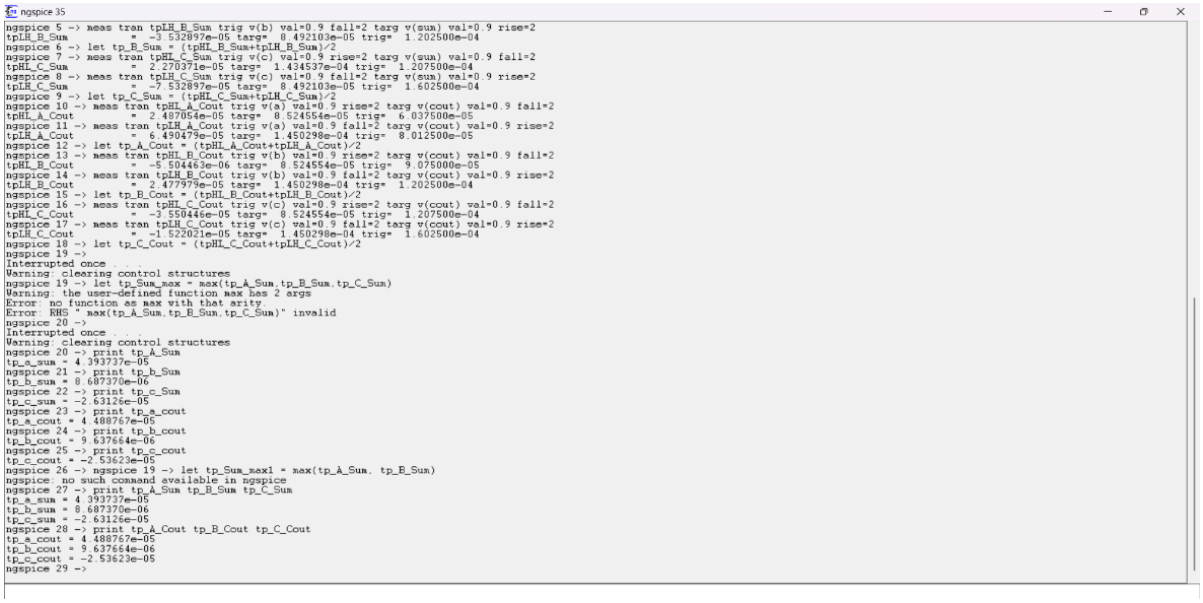
Ain	Bin	Cin	Exact Sum	Exact Cout	Approximate Sum	Approximate Cout
0	0	0	0	0	1 ×	0 ✓
0	0	1	1	0	1 ✓	0 ✓
0	1	0	1	0	1 ✓	0 ✓
0	1	1	0	1	0 ✓	1 ✓
1	0	0	1	0	1 ✓	0 ✓
1	0	1	0	1	0 ✓	1 ✓
1	1	0	0	1	1 ×	0 ×
1	1	1	1	1	0 ×	1 ✓

Results:

NGSPICE Outputs: Inputs a,b,c and Outputs approximate sum and approximate carry



Propagation Delay Using NGSPICE:



Overall Propagation Delay:

Maximum Delays:

- tp_Sum_max = max(4.393737e-05, 8.687370e-06, -2.63126e-05)

tp_Sum_max = 4.393737e-05

- tp_Cout_max = max(4.488767e-05, 9.637664e-06, -2.53623e-05)

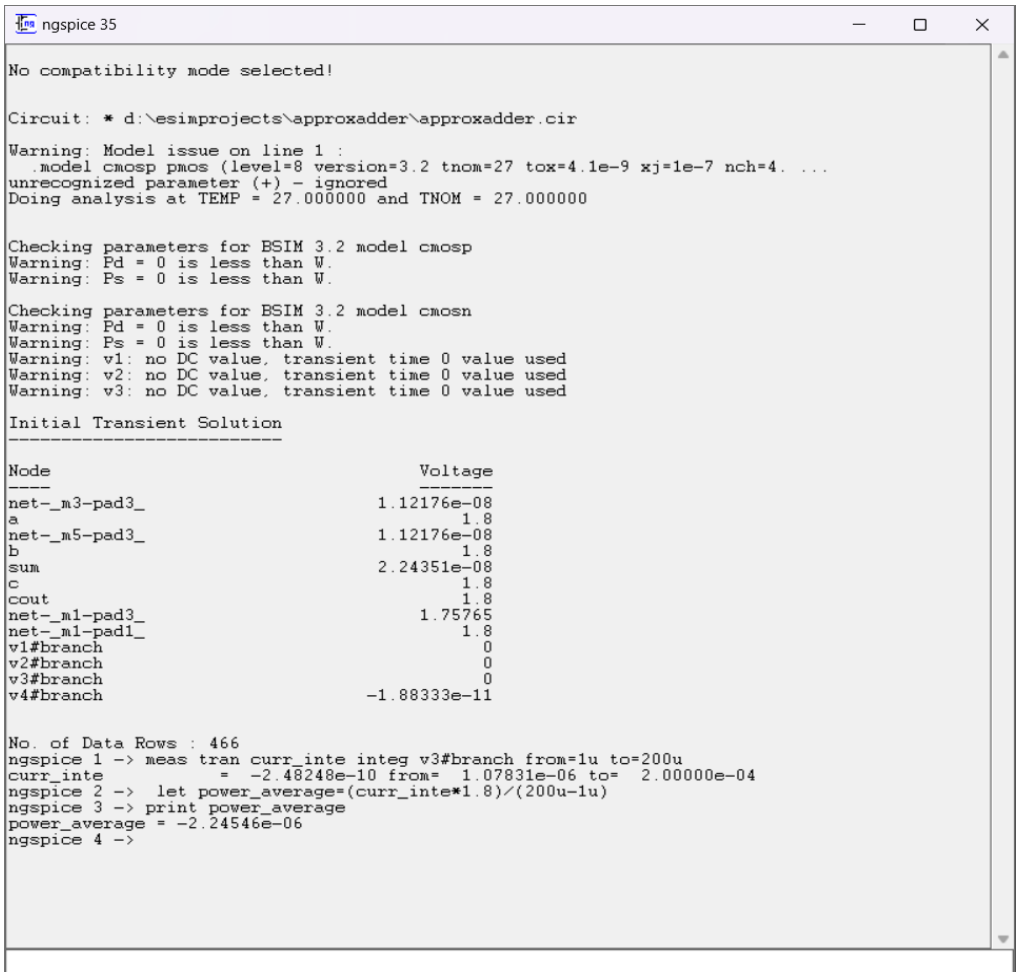
Overall Propagation Delay:

- tp_overall = max(tp_Sum_max, tp_Cout_max)

  = max(4.393737e-05, 4.488767e-05)

Overall Delay = 4.488767e-05 seconds

Average Power using NGSPICE:



References:

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3.Project tutorials: https://youtube.com/playlist?list=PL0E9jhuDlj9r-XIIgx5PPJpogx7ThS5CB&si=FOjbl6b--Gh2Ag4q

4.Delay calculation for full adder circuit: https://community.cadence.com/cadence_technology_forums/f/custom-ic-design/29194/delay-calculation-for-full-adder-circuit

5. CMOS Full Adder: https://www.youtube.com/watch?v=AXU_J4wr_yA