

# Design and Verification of Low Power SRAM using 8T SRAM Cell Approach

Athish I.S

## Abstract

The paper discusses the stability challenges of SRAM cells in advanced technology nodes, particularly due to variability and decreasing power supply voltages. Conventional 6T SRAM cells suffer from noise-related issues, especially during the read operation, which reduces stability. To address this, various alternative SRAM designs such as 8T, 9T, and 10T have been explored. This paper proposes a novel 8T SRAM topology that significantly enhances **cell stability** and **reduces power consumption**. The proposed design achieves **twice the Read Static Noise Margin (SNM)** compared to the conventional 6T SRAM cell. The modifications aim to improve performance in **low-power applications**, making the design more robust against bitline leakage noise.

**Keywords:** Read-Static Noise Margin (SNM), Stability, Power Consumption, CMOS logic, VLSI.

## 1 Circuit Details

The 8T SRAM (Static Random Access Memory) cell is an improved version of the conventional 6T SRAM, designed to enhance read stability and reduce power consumption. It consists of two main sections: the core storage unit (6T SRAM cell) and an additional read circuit (2 extra transistors) that isolates the read and write operations.

The core storage unit is composed of two cross-coupled inverters (formed by transistors M2, M5 and M3, M4) that store a single bit of data. These inverters create a bistable latch, meaning they maintain a stable value of either 0 or 1 unless externally modified. The storage nodes are labeled as Q and Qbar, where Q holds the actual stored bit, and Qbar is its complement. To allow external access to this stored data, two access transistors (M1 and M8) are used. These are controlled by the Word Line (WL), which determines when the cell is accessible for read and write operations. When  $WL = 1$ , M1 and M8 connect the storage nodes to the bitlines (BL and BLB), allowing data transfer, while when  $WL = 0$ , the storage state is isolated, ensuring the stored bit remains unchanged.

In a conventional 6T SRAM cell, reading is done by precharging the bitlines and then enabling WL, but this method introduces read noise, as it directly interferes with the storage nodes. This can cause read disturb errors, where the stored value unintentionally flips due to voltage fluctuations on Q and Qbar. To mitigate this, the 8T SRAM cell includes a separate read circuit, formed by two

additional transistors (M9 and M10). These transistors create a dedicated read path controlled by the Read Word Line (RWL) and its complement (RWLBar). During a read operation,  $RWL = 1$  activates M9 and M10, allowing the stored value at Qbar to be transferred to the Read Bitline (RBL). Since Qbar is not directly connected to BL or BLB, this method isolates the read operation from the main storage cell, preventing read noise from affecting the stored bit and improving Read Static Noise Margin (RSNM).

During a write operation,  $WL = 1$ , enabling M1 and M8 to pass data from BL and BLB to Q and Qbar. The new data is forced into the cross-coupled inverters, flipping the stored bit if necessary. Once  $WL = 0$ , the inverters hold the newly written value. The bitlines (BL and BLB) are used only during the write operation, whereas the read operation is handled exclusively by RBL, ensuring that the bitlines do not interfere with stored data during read cycles.

By separating the read and write operations, the 8T SRAM cell significantly reduces bitline leakage and read disturbance, making it ideal for low-power applications, such as IoT devices, embedded systems, and battery-operated electronics. Additionally, this design eliminates the need for precharge circuits and sense amplifiers, further reducing power consumption and improving speed. Overall, the 8T SRAM architecture offers better stability, lower power dissipation, and improved reliability compared to conventional 6T SRAM cells.

## 2 Implemented Circuit

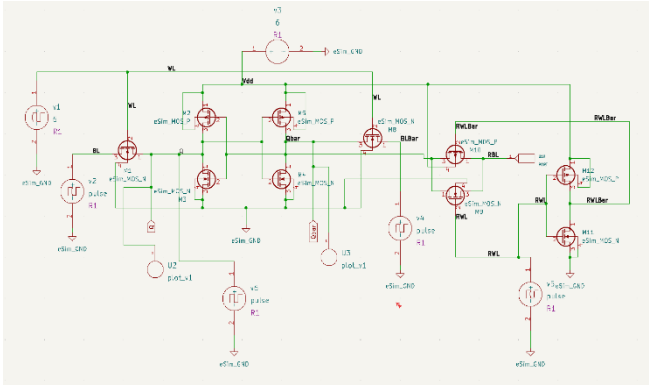


Figure 1: Implemented circuit diagram.

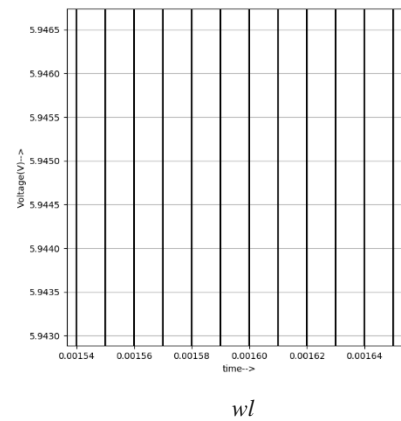
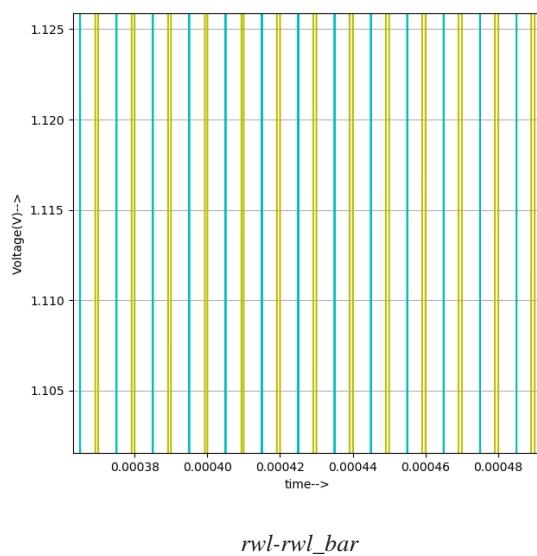
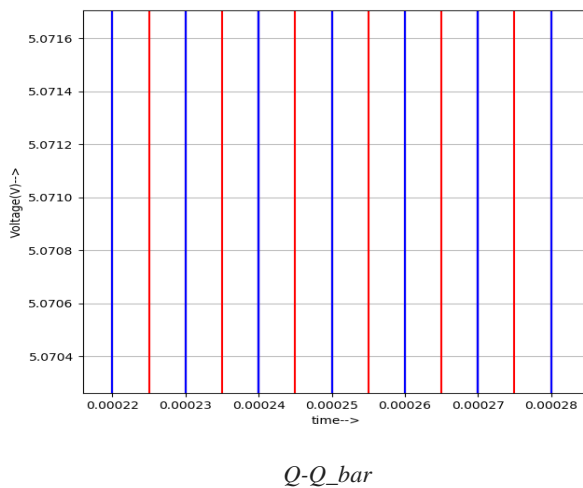


Figure 2: Implemented waveform.

### 3 Implemented Waveforms



## 4 References

- [1] Nahid Rahman, B.P. Singh, "Design and Verification of Low Power SRAM Using 8T SRAM Cell Approach, " International Journal of Computer Applications (0975 – 8887), Volume 67, No.18, April 2013.