Design and Implementation of an Efficient Ternary Comparator using FOSSEE eSim

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***Abstract*—Binary comparators, which are heavily used in digital circuits, have interconnect complexity and associated overheads such as power-delay product (PDP), parasitics, and heat hotspots. Ternary logic, or base-3, is a promising alternative that reduces interconnect complexity and improves reliability. This proposal designs and implements a scalable, low-power, and high-speed ternary comparator.**

Keywords

Double pass-transistor logic (DPL) ,Power-delay-product (PDP), Negative Ternary Inverter (NTI),Positive Ternary Inverter (PTI),Simple Ternary Inverter (STI), Piecewise Linear (PWL)

Introduction

Binary comparators are critical components in digital circuits, yet they suffer from interconnect complexity and related issues such as parasitics and heat hotspots. Ternary logic offers an efficient alternative, reducing interconnect complexity and improving overall reliability. This paper discusses the design and implementation of a ternary comparator using FOSSEE eSim.

Designing Process

Technology Node Selection

The circuit was designed based on a 32nm CMOS process. The design will be translated to a 130nm CMOS technology node in order for it to meet the new PDK.

Schematic Design

The designer will first re-create the 1-trit ternary comparator using the new circuit design software. This will mainly consist of designing the PTI, NTI, and STI circuits with NMOS and PMOS transistors as described in the original circuit descriptions. Voltage levels for ternary logic will be set to 0V, 0.5V, and 1.0V, scaled appropriately for the 130nm node.

Simulation

Transient and DC simulations will be performed to validate the circuit's functionality and ensure the correct ternary logic behavior. Piecewise Linear (PWL) inputs will be used to dynamically test all possible input combinations for the comparator.

Scaling to 4-Trit Comparator

Extend the 1-trit comparator design to a 4-trit comparator, following the same modular approach used in the original design.

Working Principle

The ternary comparator compares two ternary numbers, producing three outputs: "Greater," "Equal," and "Smaller." These outputs are realized using DPL-based logic gates. The PTI, NTI, and STI circuits process the ternary input levels to generate the necessary logic for each comparison condition. The modular design ensures scalability to higher trit counts, such as the 4-trit comparator described in the original paper.

Expected Outcome

The recreated design is expected to function identically to the original, demonstrating efficient comparison of ternary inputs. Simulation results will validate its performance, including metrics such as propagation delay, power consumption, and power-delay product, optimized for the 130nm technology node.

References

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