# Circuit Simulation Project

https://esim.fossee.in/circuit-simulation-project

**Name of the participant : Aryaman Upadhyaya**

**Title of the circuit : Low-Power CMOS Operational Amplifier Design**

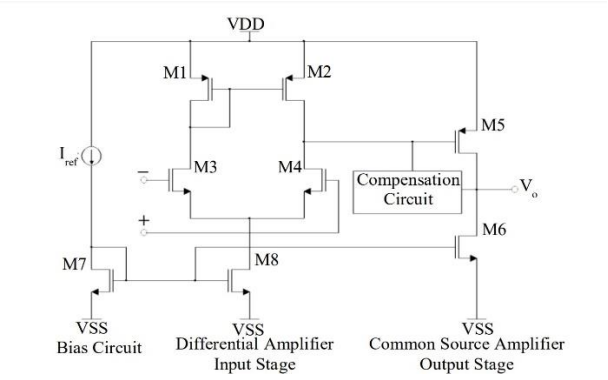
**Theory/Description : Operational amplifiers (op-amps) are important for tasks like signal amplification, filtering, and other analog operations. They are widely used in modern devices such as portable electronics, biomedical tools, and IoT systems, where saving power is essential. This project focuses on designing a low-power, two-stage CMOS op-amp with high gain, wide bandwidth, and good stability.**

**Key Features:**

- **Differential Input Stage: Ensures high input impedance and better signal rejection.**
- **Cascoded Current Mirror Load: Increases gain in the input stage.**
- **Second Gain Stage: Amplifies the signal further with a high-impedance load.**
- **Miller Compensation: Improves stability with good phase margin.**
- **Low-Power Biasing: Keeps power consumption low by reducing current usage.**

**The goal is to achieve an open-loop gain of over 70 dB, a bandwidth above 1 MHz, and power usage below 1 mW at a ±1.8 V supply voltage.**

**Circuit Diagram(s) :**



**Results (Input, Output waveforms and/or Multimeter readings) :**

**Expected simulation results include:**

- **DC Analysis: Proper biasing at all nodes with expected voltage levels.**
- **AC Analysis:**
  - **Open-loop gain >70 dB.**
  - **Unity-gain bandwidth >1 MHz.**
  - **Phase margin >60 degrees.**
- **Transient Analysis: Clean step response with minimal overshoot and fast settling time.**
- **Power Analysis: Total power consumption <1 mW.**

**These results will be validated using simulations in eSim, with waveforms showing input-output relationships and multimeter readings confirming biasing and power levels.**

**Source/Reference(s) :**


1. **Razavi, B. (2001).** ***Design of Analog CMOS Integrated Circuits.***
2. **IEEE Transactions on Circuits and Systems: Research articles on low-power CMOS op-amp design.**