Research Migration Project

https://esim.fossee.in/research-migration-project

The Research Migration Project is an initiative of FOSSEE, IIT Bombay that promotes the use of eSim for reproducing published research circuits originally implemented using proprietary simulation tools. The objective is to migrate these validated designs to eSim to build an open source resource database.

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Title of the circuit: Simulation of a Fault-Tolerant Full Adder using Double-Pass CMOS Transistors Using eSim

Theory/Description: A full adder is a basic digital circuit that adds three one-bit inputs, A, B and Cin, and produces Sum and Cout. The proposed work focuses on migrating a published self-checking fault-tolerant full-adder architecture based on Double Pass Transistor Logic and two-rail encoding, including its fault-detection mechanism. The circuit provides differential outputs and is designed to detect errors caused by transient faults during operation. The proposed design uses 20 transistors and is intended to provide reliable addition with reduced transistor count.

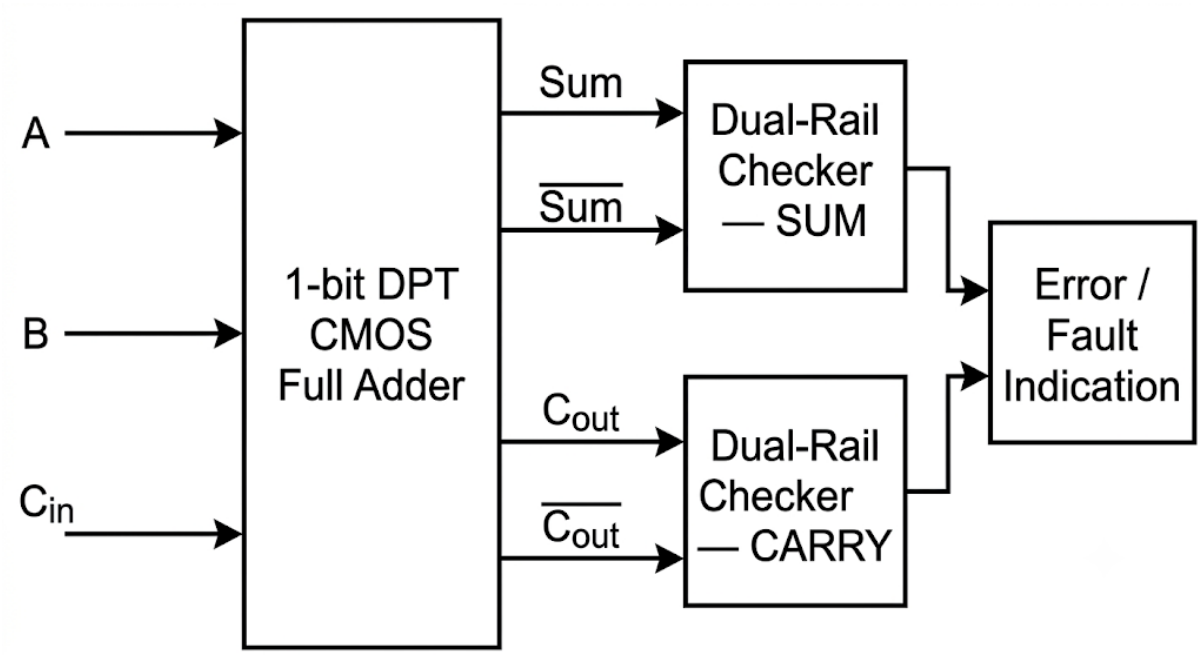
Reason to reproduce with eSim : The circuit is suitable for reproduction in eSim because it is a transistor-level CMOS circuit that can be simulated using SPICE. eSim is an open-source EDA tool using Ngspice for circuit simulation. Reproducing this circuit will provide an open-source implementation of a published fault-tolerant circuit and will allow its normal operation and fault-detection behaviour to be verified.

Expected Outcome/Outputs: The proposed circuit will be implemented in eSim at the transistor level using the Double Pass Transistor Logic (DPL) full-adder architecture, and its functionality will be verified through exhaustive input combinations of A, B, and Cin corresponding to the full truth table of a 1-bit adder. During normal operation, the complementary outputs (Sum/Sum_b and Cout/Cout_b) will be monitored in transient analysis to confirm correct dual-rail behaviour, ensuring that each logic ‘1’ is represented by a valid differential pair and each logic ‘0’ by its complement. After validating fault-free operation, a deliberate transient or stuck-at fault will be injected at one of the input nodes or internal transistor nodes to emulate a real hardware failure scenario. The response of the circuit will then be observed, where the dual-rail checker is expected to detect the violation of the complementary relationship between output pairs and generate a fault indication signal. The resulting waveforms will clearly demonstrate normal switching behaviour, followed by

corruption under fault injection, and finally activation of the checker output, thereby validating both the correctness and the self-checking capability of the proposed fault-tolerant full adder.

Circuit Diagram(s) :

Block Diagram(s):



Expected Results (Input, Output waveforms and/or Multimeter readings):

The inputs A, B and Cin are applied as digital signals, where logic '0' corresponds to 0 V and logic '1' corresponds to VDD (typically 1.8 V or 3.3 V in simulation). The circuit produces dual-rail outputs for Sum and Carry (Sum/Sum_b and Cout/Cout_b), which are designed to be complementary in normal fault-free operation. For all input combinations from 000 to 111, the circuit is expected to follow the standard full adder truth table, and the self-checking full adder based on two-rail encoding scheme should maintain correct logical complementarity as per the design of the Double Pass Transistor logic.

When a fault is added (like a short glitch at an input or internal node), this complementary behavior will break. Sum will no longer match Sum_b, or Cout will not match Cout_b. The dual-rail checker will detect this mismatch and give a fault signal.

In simulation, we should see normal clean switching waveforms when there is no fault. When the fault is injected, there will be a visible disturbance in the output waveforms and the checker output will respond immediately. We may also notice small changes or spikes in current during the fault event, which helps us study how the circuit reacts in eSim**.**

Research Paper/Journal/etc.

Title : A Fault-Tolerant Full Adder in Double Pass CMOS Transistor

Pages: 36–40

Author: Abdelmonaem Ayachi, Belgacem Hamdi

Link:https://publications.waset.org/10003320/a-fault-tolerant-full-adder-in-double-pass-cmos-transistor

Source/Reference(s):

[1] A. Ayachi and B. Hamdi, "A Fault-Tolerant Full Adder in Double Pass CMOS Transistor," International Journal of Electronics and Communication Engineering, vol. 10, no. 1, pp. 36–40, 2016.
