CHENNAI INSTITUTE OF TECHNOLOGY
(Autonomous)

Power Optimization of 8:1 MUX using Transmission Gate Logic (TGL) with Power Gating Technique

Name of the Participant: Ragul T

Project Guide: Dr.R.M Bommi

Institute: Chennai Institute of Technology (CIT)

University: Anna University

Problem Statement:

Design an optimized 8:1 MUX using Transmission Gate Logic (TGL) combined with Power Gating techniques to reduce power consumption

Theory/Description:

This paper focuses on reducing power dissipation in an 8:1 multiplexer designed with Transmission Gate Logic (TGL) using the Power Gating Technique. The design reduces leakage power and current during active mode by utilizing the Power Gating approach, with PMOS and NMOS transistors connected for strong output levels. The simulation of this design was done using eSim in a 90nm technology node, achieving a 36% reduction in leakage current and a 43% reduction in leakage power. The results show a power reduction of 4.021fW, a current reduction of 7.381pA, and a supply voltage of 0.7V.

Circuit Diagram:

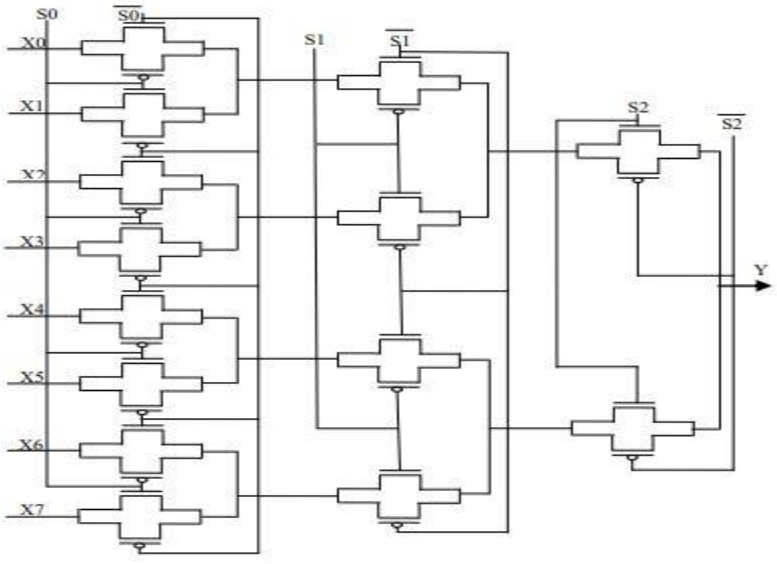

Fig.1 8:1 MUX

Application:

- **Low-Power VLSI Design**: This technique is ideal for low-power systems, particularly in embedded devices and IoT applications where power efficiency is critical.

- **Mobile Devices**: Optimizing power consumption in multiplexers used in mobile and wearable devices, extending battery life.
- **Space and Aerospace Electronics**: Suitable for circuits in aerospace applications, where minimizing power consumption and heat dissipation is crucial for system reliability.
- **Power-Optimized Circuitry**: Can be applied to other digital circuits, such as multiplexers, adders, and logic gates, to reduce energy consumption in high-performance computing systems.

Reference:

Title of the paper: Power Optimization of 8:1 MUX using Transmission Gate Logic (TGL) with Power Gating Technique

Link: https://citeseerx.ist.psu.edu/document?repid=rep1&type=pdf&doi=07ca738c7a654909b679b96d74402f9d096566a0