Research Migration Project

https://esim.fossee.in/research-migration-project

The Research Migration Project is an initiative of FOSSEE, IIT Bombay that promotes the use of eSim for reproducing published research circuits originally implemented using proprietary simulation tools. The objective is to migrate these validated designs to eSim to build an open source resource database.

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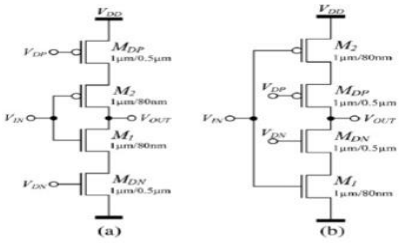
Title of the circuit : Design and Simulation of a Tunable Low-Power CMOS Delay Line Using Current-Straved Inverter Cells in eSim.

Theory/Description : The proposed circuit is based on a current-starved CMOS inverter, where additional MOS transistors control the current available for charging and discharging the inverter output. This controlled current determines the propagation delay of the inverter. By varying the control/bias voltage, the propagation delay can be tuned. Multiple current-starved inverter cells are connected in cascade to form a multi-stage tunable delay line. The circuit will be simulated in eSim using transient analysis to study its delay characteristics, control-voltage dependence, and power consumption.

Reason to reproduce with eSim : This circuit is suitable for eSim because it can be easily simulated and analyzed using its open-source platform. eSim allows verification of the delay, output waveforms, and power consumption at different control voltages. It also provides a useful and cost-effective way to understand and reproduce the tunable CMOS delay line.

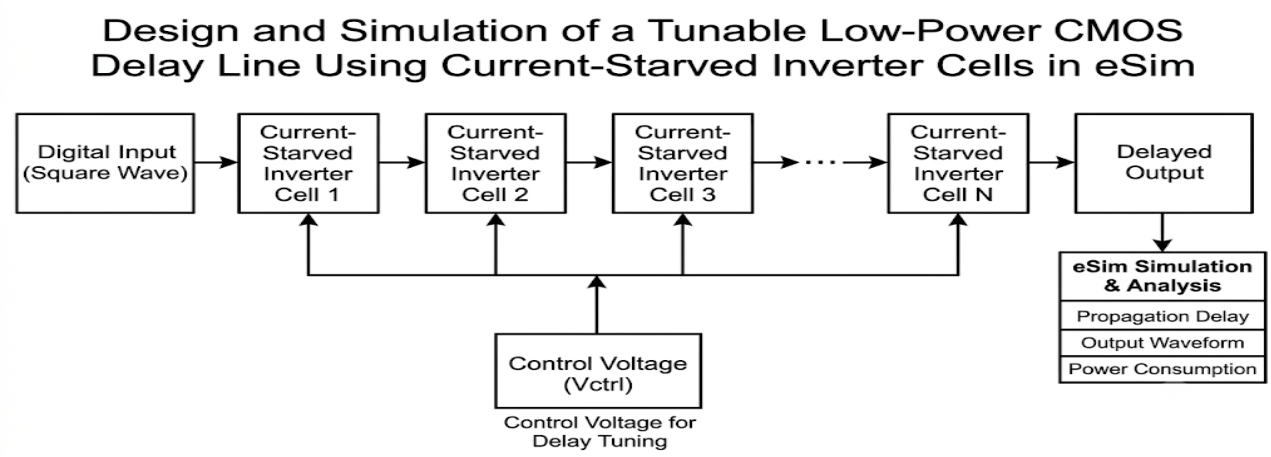
Expected Outcome/outputs : The circuit is expected to produce a tunable delay by controlling the current in the inverter cells. In eSim, the delay, output waveform, and power consumption can be measured at different control voltages. The performance is validated by comparing the simulated delay with the expected results.

Circuit Diagram(s) :



Schematic diagrams of the delay gates with two complementary current limiting transistors M_{DN} and M_{DP}: (a) CSI variant, (b) OSI variant.

Block Diagram (s) :



Expected Results (Input, Output waveforms and/or Multimeter readings) : The circuit is expected to accept a digital square-wave input and produce a similar square-wave output with a controlled propagation delay. By varying the control voltage of the current-starved inverter cells, the charging and discharging current changes, which in turn changes the delay of the output signal. During simulation in eSim, the input and output waveforms, propagation delay, voltage levels, current, and power consumption can be observed and measured. The results can be validated by comparing the measured delay and output waveform with the expected theoretical behavior.

Research Paper/Journal/etc. : Przemysław Mroszczyk and Piotr Dudek, "Tunable CMOS Delay Gate With Improved Matching Properties," *IEEE Transactions on Circuits and Systems I: Regular Papers*, Vol. 61, No. 9, pp. 2586–2595, 2014. DOI: 10.1109/TCSI.2014.2312491.

This paper is directly related to tunable CMOS delay gates and current-starved inverter (CSI) based delay lines, making it relevant to the proposed low-power CMOS delay line project.

Title : "Tunable CMOS Delay Gate With Improved Matching Properties,"
Author : Przemysław Mroszczyk and Piotr Dudek
Page No. : (Page numbers, if available)
Link : https://ieeexplore.ieee.org/document/6807526

Source/Reference(s)

- IEEE Xplore – "Tunable CMOS Delay Gate With Improved Matching Properties"
- eSim Documentation – Circuit simulation and analysis
- Sedra/Smith, *Microelectronic Circuits* – CMOS inverter and MOSFET fundamentals

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