FOSSEE eSim - Research Migration Project

Project Proposal / Approval Document

Name of the participant	KAMINENI NAGA SUDEERGA
Affiliation / Institution	Rajiv Gandhi University of Knowledge Technologies, Nuzvid
Title of the circuit	Design and Transistor-Level Analysis of a Reconfigurable Low-Power 4-bit Array Multiplier Using Hybrid PTL-CMOS Logic

1. Theory / Description

The proposed circuit is a 4-bit binary array multiplier that accepts two 4-bit inputs and produces an 8-bit product. The multiplier first generates partial products using AND operations. These partial products are then added through an array of half-adders and full-adders. To investigate low-power digital VLSI design, selected logic cells are implemented using a Hybrid Pass-Transistor Logic (PTL)-CMOS approach. The design will be evaluated at transistor level in eSim for correct logic operation and performance.

2. Reason to Reproduce / Implement with eSim

eSim provides an open-source environment for schematic capture and circuit simulation. The proposed design is suitable for eSim because its individual CMOS/PTL logic cells, adder stages, partial-product generation and complete multiplier can be verified through simulation. The project also provides educational value by connecting digital multiplication with transistor-level CMOS design and measurable power/delay analysis.

3. Block Diagram

4-bit Input A	4-bit Input B
|	|
+------ Partial Product Generation ------ +	
|	
Array of Half/Full Adders	
|	
8-bit Product P[7:0]	

4. Circuit Diagram / Proposed Schematic Structure

The detailed schematic will consist of 16 partial-product generation cells, half-adder and full-adder cells arranged as a 4 x 4 multiplier array, and Hybrid PTL-CMOS implementations for selected logic functions. Each cell will be labelled with its inputs, outputs, supply voltage and transistor connections. The final detailed schematic will be produced during eSim implementation.

A[3:0] x B[3:0]	->	16 partial products	->	Adder array	->	P[7:0]
AND/logic cells		HA/FA stages		Hybrid PTL-CMOS		8-bit output

5. Expected Outcome / Outputs

- Correct 4-bit x 4-bit multiplication for representative input combinations.

- An 8-bit product output waveform that agrees with the expected binary multiplication result.

- Functional verification of the partial-product and adder stages.

- Transistor-level simulation results for the Hybrid PTL-CMOS implementation.

- Measured power consumption and propagation delay, where supported by the simulation setup.

- Power-delay product (PDP) and transistor-count comparison with a conventional CMOS implementation, if both versions are implemented.

6. Expected Results (Input / Output Waveforms)

Example functional checks: A=0011 and B=0010 should produce P=00000110; A=0101 and B=0011 should produce P=00001111. Input signals will be applied as digital voltage waveforms and the output P[7:0] will be observed in the simulator. Power and delay values will be recorded from the final simulation rather than assumed in advance.

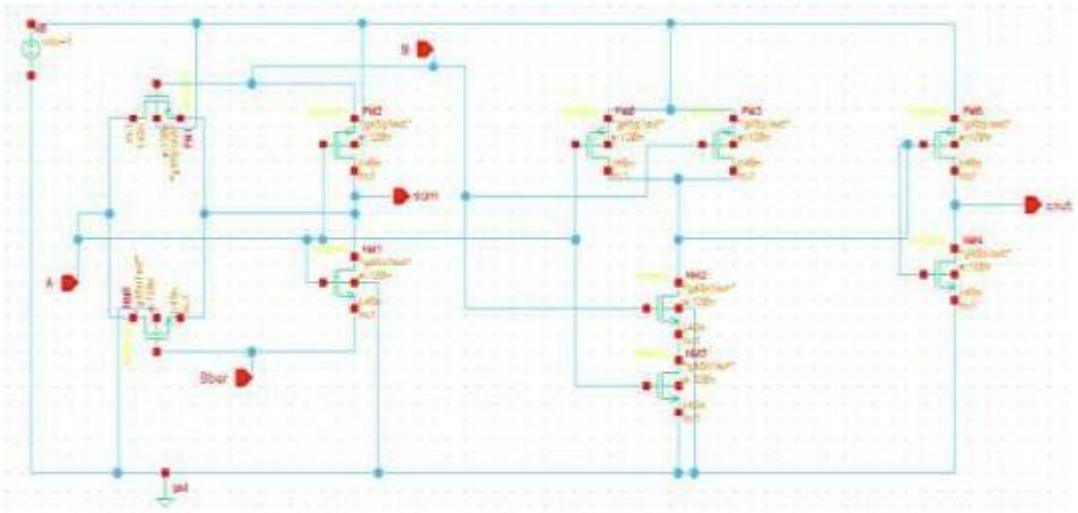

Figure 1 :Half Adder

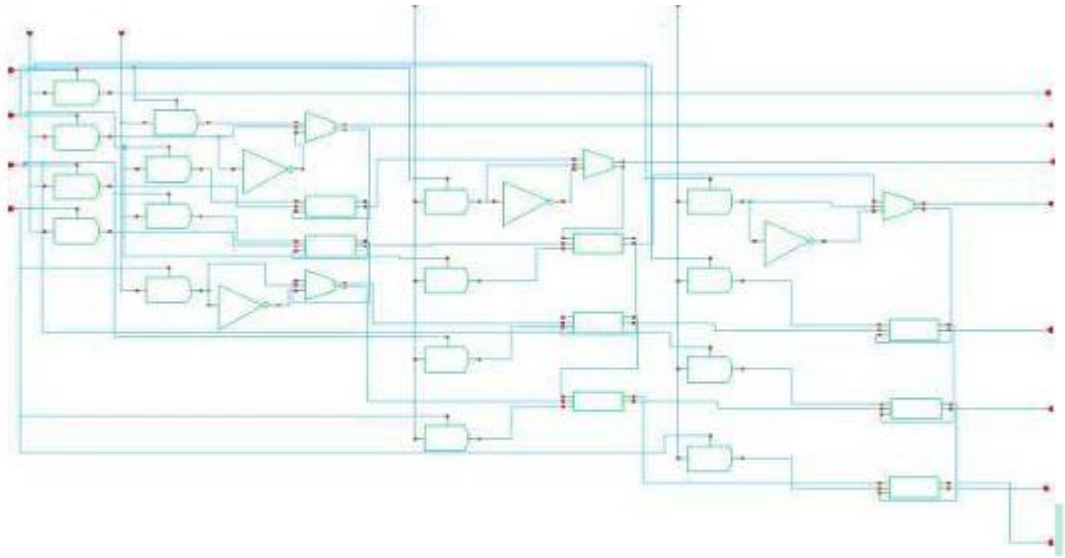

Figure 2 : Schematic of 4-bit Array Multiplier using hybrid PTL and CMOS logic, showing partial product generation and adder network.

7. Research Paper / Journal Reference

The FOSSEE Research Migration Project template requires at least one directly relevant research paper, journal article or patent. **Title:** Low-Power 4-bit Array Multiplier Using Hybrid PTL-CMOS
Author(s): Richa Gupta Department of Electronics and Communication Engineering Maulana Azad National Institute of Technology (MANIT) Bhopal, India and Dr. Bhavana Prakash Shrivastava Department of Electronics and Communication Engineering Maulana Azad National Institute of Technology (MANIT) Bhopal, India and Dr. Laxmi Pradhan Kumre Department of Electronics and Communication Engineering Maulana Azad National Institute of Technology (MANIT) Bhopal, India
DOI: 10.1109/SCEECS68810.2026.11429765.

8. Source / Reference(s)

FOSSEE eSim Research Migration Project proposal template. The supplied template specifies the required fields for

participant/institution, circuit title, theory/description, reason for eSim, expected outcomes, circuit and block diagrams, expected results, and a mandatory relevant research reference.

Note: This is an approval draft. Final transistor values, waveforms, power, delay and detailed schematic should be filled after eSim implementation