Research Migration Project

Name of the participant :
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Title of the circuit :

Low Power CMOS Folded Electro Cascode Amplifier for Electrocardiogram (ECG) Applications

Theory/Description :

ECG signals are very weak, approximately 5 µV to 5 mV, and ECG front-end amplifiers must provide sufficient amplification while limiting noise and power consumption. The proposed circuit is a CMOS folded electro-cascode amplifier using a PMOS differential input pair, current-mirror biasing, folded-cascode stages, common-source/common-gate operation, and cascoded PMOS/NMOS devices. The reference design uses 45-nm CMOS technology, with 10 PMOS and 6 NMOS transistors and a reported 250-nA bias current.

Reason to reproduce with eSim :

The purpose is to migrate a published transistor-level CMOS analog circuit from the proprietary Cadence Virtuoso/Spectre environment to the open-source eSim environment. The migration will provide an open-source implementation for studying CMOS analog design and allow verification of DC, transient, and power characteristics. Differences caused by available device models or technology parameters will be documented rather than assuming identical results

Expected Outcome/outputs :

A functional eSim implementation of the folded electro-cascode amplifier with DC response, transient input/output waveforms, output-voltage measurements, power-consumption analysis, and comparison with the published results.

Intended supply/operation: 1.2 V

Transient input: 1.2 V

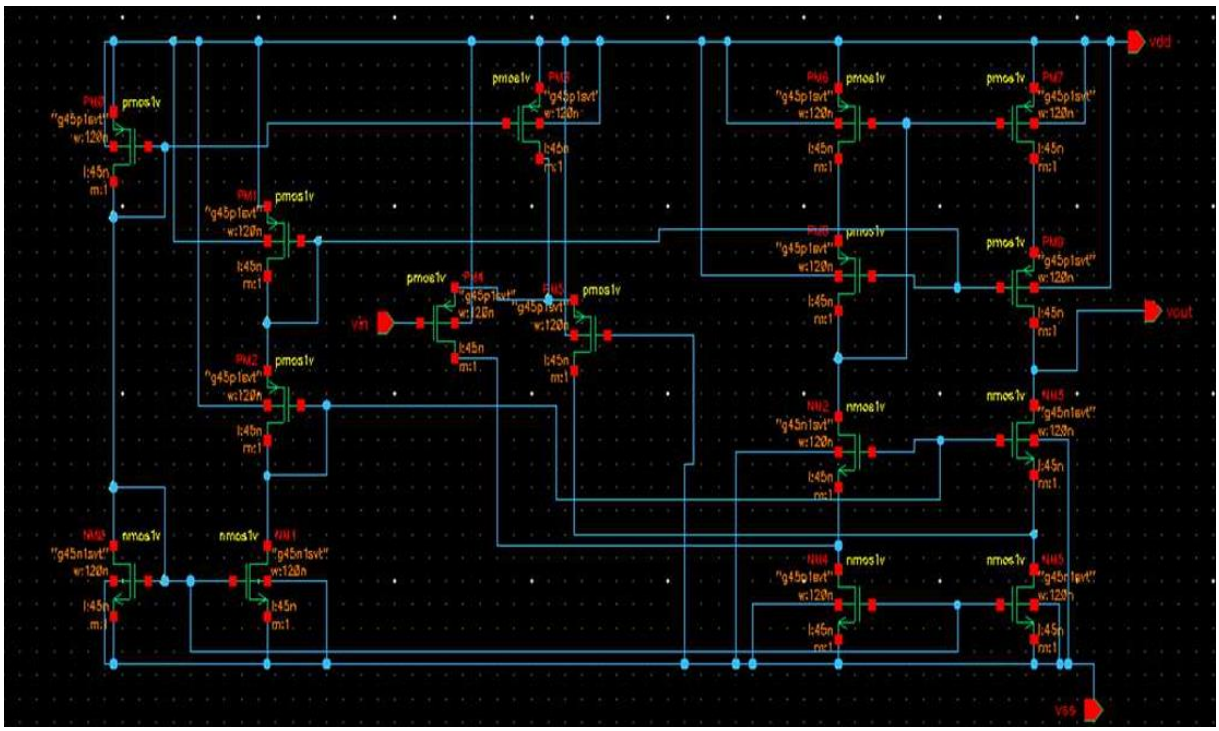
Transient output: 4.4614 V

DC input: 1.008 V

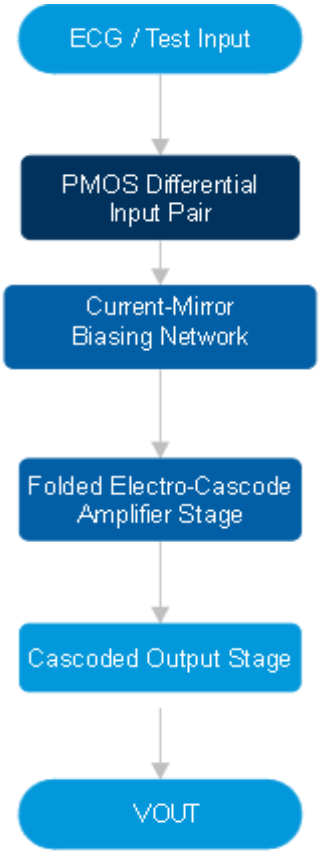
DC output: 4.442 V

Reported steady-state transient power: 2.94 mW

Circuit Diagram(s) :



Block Diagram (s) :



Expected Results (Input, Output waveforms and/or Multimeter readings) :

The eSim simulation will produce:

1.Input voltage waveform

2.Output voltage waveform

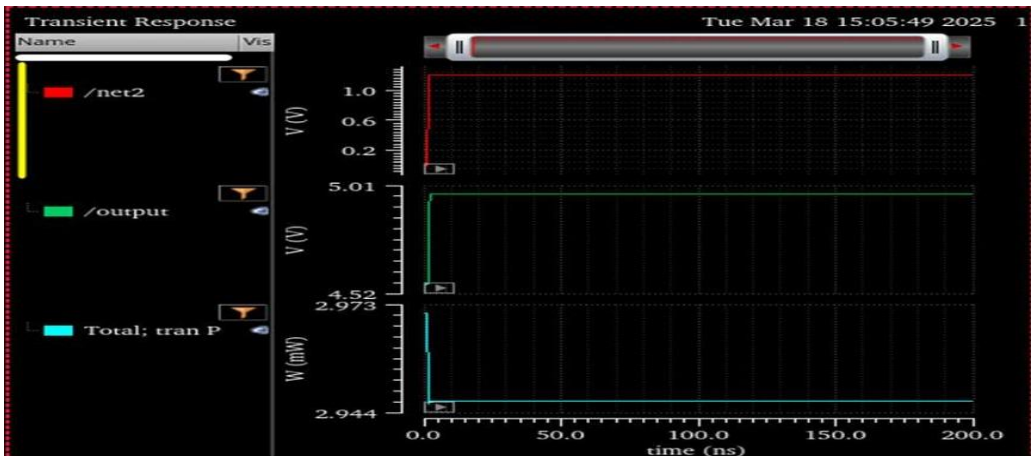
3.DC input-output transfer characteristic

4.Transient response

5.Supply/current measurement

6.Power-consumption result

Graph:



Research Paper/Journal/etc. :

Title : Low Power CMOS Folded Electro Cascode Amplifier Design

for Electrocardiogram Applications

Author : Rangeetha S; Ganesh Babu C; Bavana K B; Devadharshini M; Dharanya C.

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Link : https://ieeexplore.ieee.org/document/11019942

Source/Reference(s) :

1. Rangeetha S, Ganesh Babu C, Bavana K B, Devadharshini M, Dharanya C, Low Power CMOS Folded Electro Cascode Amplifier Design for Electrocardiogram Applications, 2025 Fourth International Conference on Smart Technologies, Communication and Robotics (STCR).

2. eSim / FOSSEE Research Migration Project guidelines.

3. Cadence Virtuoso/Spectre — original paper's design and simulation environment.

4. Suitable CMOS MOSFET models available in the eSim/Ngspice environment

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