Research Migration Project

https://esim.fossee.in/research-migration-project

The Research Migration Project is an initiative of FOSSEE, IIT Bombay that promotes the use of eSim for reproducing published research circuits originally implemented using proprietary simulation tools. The objective is to migrate these validated designs to eSim to build an open source resource database.

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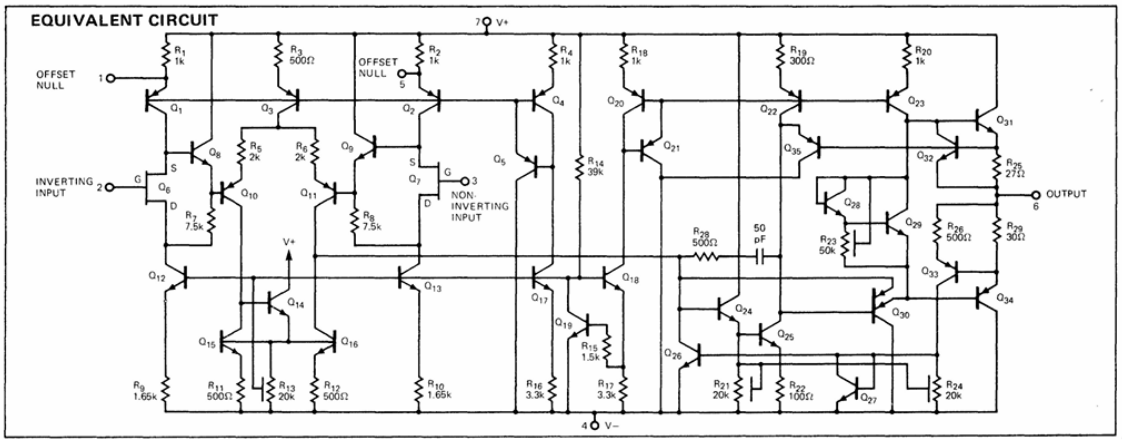
Title of the circuit : Simulation and Internal Circuit Analysis of the µA740 FET-Input Operational Amplifier

Theory/Description : The µA740 is a high-speed JFET-input operational amplifier designed to deliver exceptionally high input impedance (10^{12} Ω) and extremely low bias currents using a matched JFET differential input pair (Q6, Q7) combined with active loading and offset nulling circuitry (Q1–Q3) at pins 1 and 5. The signal is processed through an intermediate gain stage composed of bipolar transistors (Q8–Q27) that provide high voltage gain, differential-to-single-ended conversion, and frequency stability via an internal 50 pF compensation capacitor and a 500 Ω damping resistor (R28). Finally, the amplified signal is passed to a complementary push-pull output stage (Q31, Q34) equipped with current-limiting protection transistors (Q32, Q33) and resistors (R25, R29) to safely drive external loads at pin 6.

Reason to reproduce with eSim : This circuit is suitable for eSim as it allows open-source SPICE modeling and transient analysis of a discrete transistor-level FET operational amplifier like the µA740. It enables the verification of key performance parameters such as open-loop gain, input impedance, slewing behavior, and internal frequency compensation (50 pF capacitor effect) without relying on proprietary simulation software. Reproducing this design contributes a foundational, high-impedance op-amp subcircuit block to the eSim open-source resource database.

Expected Outcome/outputs : As a basic test of the project, this circuit is first implemented in the voltage follower (unity-gain buffer) configuration to verify correct functioning of the transistor-level model before proceeding to detailed analysis. The eSim simulation will produce transient response voltage waveforms showing signal amplification and AC frequency response plots (magnitude and phase vs. frequency) of the transistor-level µA740 op-amp circuit. Key outputs will include the determination of open-loop voltage gain, 3 dB bandwidth, unity-gain bandwidth, and slew rate. Additionally, the results will verify the stabilizing effect of the internal 50 pF frequency compensation capacitor and validate the high-impedance, low-bias-current behavior of the JFET input stage against standard datasheet parameters.

Circuit Diagram:



Source/Reference(s):

[1] Texas Instruments, *μA740 FET-Input Operational Amplifier Datasheet*, Texas Instruments Inc., USA.

[2] Fairchild Semiconductor, *μA740 High-Speed FET-Input Operational Amplifier Datasheet*, Fairchild Semiconductor Corporation.

[3] P. R. Gray, P. J. Hurst, S. H. Lewis, and R. G. Meyer, *Analysis and Design of Analog Integrated Circuits*, 5th Edition, Wiley, 2009.