# eSim Research Migration Proposal Synopsis

eSim Semester Long Internship - Autumn 2026 | Screening Task 1

**TASK 1: RESEARCH MIGRATION**

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| **Project Title:** | **Simulation and Transient Analysis of a 60-Gb/s 1:4 Demultiplexer in 22-nm CMOS Using TSPC Logic** |
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| **Institution / Degree:** | Rajiv Gandhi University of Knowledge Technologies, Nuzvid \| B.Tech in Electronics and Communication Engineering |
| **Reference Paper:** | *"60-Gb/s 1:4 Demultiplexer in 22-nm FD-SOI Technology Using TSPC Logic: A Circuit-to-System-Level Analysis and Design"*<br>**Authors:** Babak Sadiye, Mohammed Iftekhar, Wolfgang Mueller, and J. Christoph Scheytt<br>**Source:** IEEE Transactions on Very Large Scale Integration (VLSI) Systems, Vol. 34, No. 2, pp. 366–378, Feb. 2026 \| **DOI:** 10.1109/TVLSI.2025.3625787 |

## 1. PROJECT OVERVIEW & MOTIVATION

In high-speed wireline receiver front-ends, serial-to-parallel conversion is essential to interface gigabit serial data streams with digital processing blocks. While conventional Current-Mode Logic (CML) flip-flops suffer from substantial static power dissipation and narrow output swing, True Single-Phase Clock (TSPC) dynamic logic offers single-phase clock routing, minimal transistor count, full rail-to-rail voltage swing, and purely dynamic switching power ($P \propto f \cdot V_{DD}^2$). This project aims to implement and simulate the complete 60-Gb/s 1:4 binary-tree demultiplexer architecture in eSim, resolve timing race conditions, and validate dip-free dynamic switching performance.

## 2. CIRCUIT HIERARCHY & SUB-BLOCKS TO IMPLEMENT IN ESIM

### Block A: Pulse-Shaped TSPC D-Flip-Flop (DFF)

- **Core Logic:** 3-stage cascaded gated inverter architecture ($P_{1-4}, N_{1-5}$).
- **Dip Suppression Network:** 4-transistor asymmetric pulse shaper ($P_5, N_6, P_6, N_7$) delaying the rising edge by one inverter delay while maintaining instantaneous falling response to eliminate output voltage dips during long zero-sequences.

### Block B: TSPC Dynamic Latch & Prescaler

- **Dynamic Latch:** Low-transistor-count gated dynamic latch configured to align and synchronize parallel branch outputs.
- **Divide-by-2 Frequency Prescaler:** TSPC-based regenerative frequency divider generating a synchronous half-rate clock ($ ext{CLK}/2$) for second-stage demultiplexing.

### Block C: 1:2 Sub-Stage & Top-Level 1:4 Binary-Tree Demultiplexer Architecture

- **1:2 DEMUX Block:** Dual-branch configuration pairing a direct DFF path with a synchronized DFF + Latch path.
- **Top-Level 1:4 DEMUX Tree:** Cascaded 2-stage binary architecture driving 4 parallel output streams ($D_0, D_1, D_2, D_3$) from high-speed serial bit sequences with integrated clock buffer distribution.

## 3. SIMULATION METHODOLOGY & VERIFICATION BENCHMARKS

- **Transient Operational Verification (`.tran`):** Capture and verify complete serial-to-parallel bit deserialization across multi-gigabit data streams (PRBS patterns) in eSim.
- **Voltage Dip Mitigation Analysis:** Demonstrate elimination of spurious output voltage dips by comparing internal node voltages ($A, B,  ar{Q}$) in standard vs. pulse-shaped TSPC DFFs.
- **Timing Margins & Parameter Sweeps:** Characterize setup time, hold time, and clock-to-Q propagation delays across varying supply voltages ($0.6 ext{ V}$, $0.8 ext{ V}$, $1.0 ext{ V}$, and $1.2 ext{ V}$).
- **Dynamic Power Characterization:** Validate the linear scaling of power with data rate ($P \propto f$) and quadratic scaling with supply voltage ($P \propto V_{DD}^2$).
- **EDA Tool & Device Models:** eSim v2.3 / v2.5 with Ngspice engine utilizing 22-nm Predictive Technology Models (PTM) / BSIM4 cards.

**Non-Duplication Declaration:** I hereby declare that this research migration project and the referenced IEEE paper have not been implemented or proposed under the FOSSEE Completed/In-Progress Research Migration archives, Circuit Simulation Project, or default eSim installation examples.

**Date:** August 19, 2026

**Applicant:** BALA SAMPURNA YERIGALA