DESIGN AND ANALYSIS OF A LOW-POWER RECONFIGURABLE ALU USING FINE-GRAINED CLOCK GATING

Project Report

Submitted by

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1. Research Migration Project

The Research Migration Project is an initiative of FOSSEE, IIT Bombay that promotes the use of eSim for reproducing published research circuits originally implemented using proprietary simulation tools. The objective is to migrate these validated designs to eSim to build an open-source resource database

2. Title of the project

Design and Analysis of a Low-Power Reconfigurable ALU using Fine-Grained Clock Gating

3. Introduction

An Arithmetic Logic Unit is a fundamental digital datapath component that performs arithmetic and logical operations on binary operands.

In a reconfigurable ALU, different functional operations are selected according to an operation code. Although the ALU performs useful computation only for the selected function, unnecessary switching in inactive portions can contribute to dynamic power.

Clock gating is a widely used technique for reducing unnecessary switching by preventing clock activity from reaching inactive sequential logic. Fine-grained clock gating applies this concept at a smaller functional-block level so that only the required part of the ALU is enabled for a selected operation.

4. Objectives

The main objectives of this project are:

1. To design an 8-bit reconfigurable ALU.
2. To verify its functional behavior using simulation.
3. To establish a conventional ALU power baseline.
4. To implement and analyze fine-grained clock gating.
5. To compare power and thermal results.
6. To use the verified design as the starting point for an eSim migration after approval.

5. Theory and Description

The ALU accepts two 8-bit operands A and B, together with a 3-bit operation-select input Op. The output Y is 8 bits wide and a carry output is provided for arithmetic operations.

The design supports eight operation codes.

Table 1: ALU Operation Codes

Op[2:0]	**Operation**	**Description**
000	ADD	$A + B$
001	SUB	$A - B$
010	AND	A AND B
011	OR	A OR B
100	XOR	A XOR B
101	NOT	Bitwise NOT of A
110	Increment	$A + 1$
111	Decrement	$A - 1$

6. Architecture and Working Principle

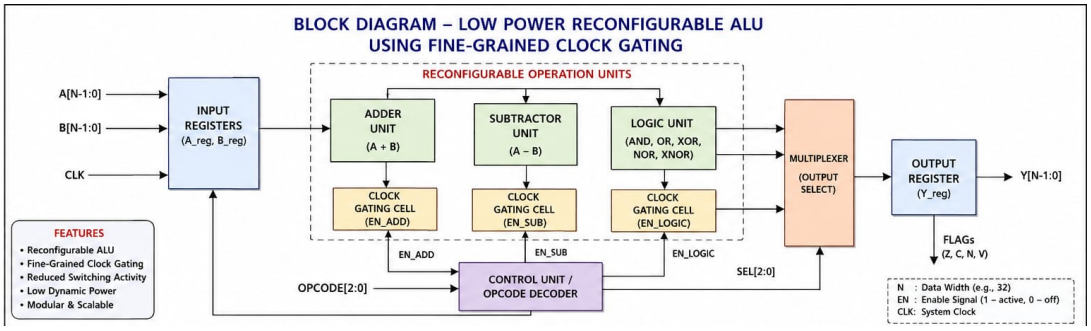
The proposed architecture divides ALU functionality into operation-related sections. The operation code determines the required computation.

Fine-grained clock-gating control is used to reduce clock activity in inactive sections. The selected section produces the ALU result, while the carry output indicates arithmetic carry where applicable.

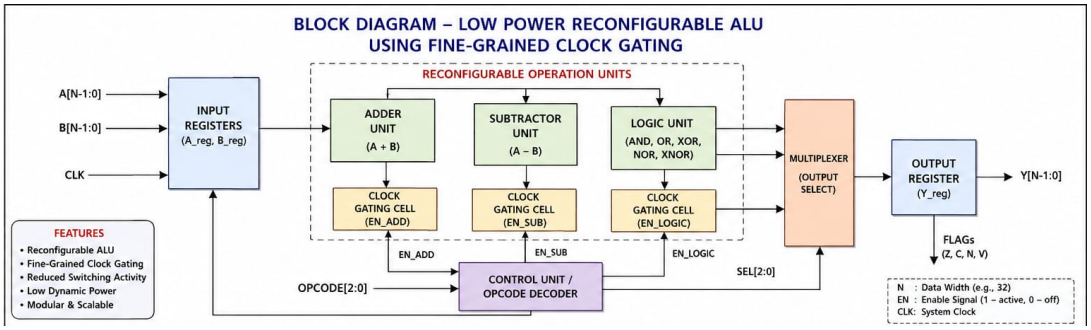
Table 2: Functional Architecture

Inputs / Control	**Functional Section**	**Outputs**
$A[7:0], B[7:0]$	Arithmetic Unit	$Y[7:0]$, carry
$Op[2:0]$	Logic Unit	$Y[7:0]$
CLK, RESET	Increment / Decrement Unit	$Y[7:0]$
Clock-gating control	Operation-specific enable	Reduced switching activity

7. Block Diagram



8. Circuit Diagram



9. Simulation and Functional Verification

A Verilog testbench was used to exercise the ALU operations.

The waveform contains the following signals:

- CLK
- RESET
- A
- B
- Op
- Y
- carry

The operation code changes across the eight functions. The final test uses

$$A = \texttt{FF}, \qquad B = \texttt{01}, \qquad Op = 000$$

which produces

$$Y = 00, \qquad carry = 1$$

This demonstrates the 8-bit addition overflow/carry condition.

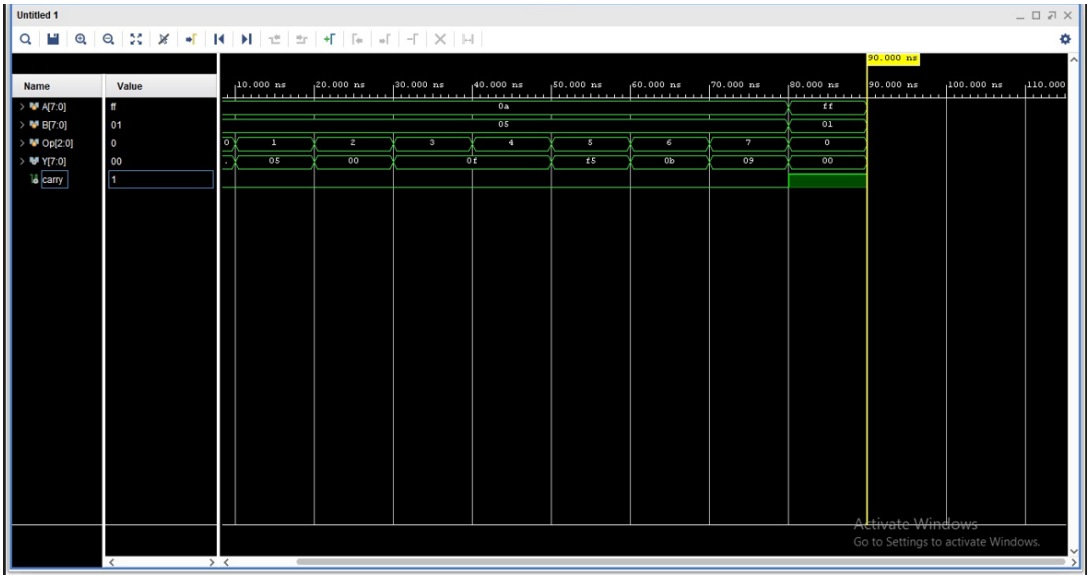


Figure 1: Vivado behavioral simulation waveform showing clock, reset, operands, operation code, result and carry.

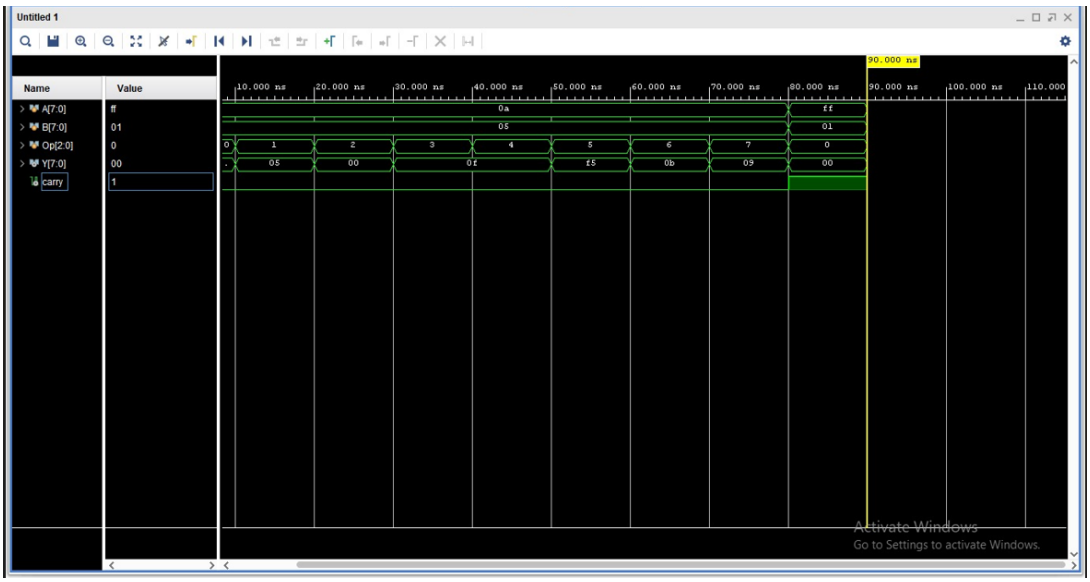


Figure 2: Zoomed waveform view highlighting the final FF + 01 test and carry = 1 condition.

10. Synthesis and Power Analysis

After functional verification, both the conventional and clock-gated ALU designs were synthesized and analyzed in Vivado.

The reported estimates are based on the synthesized design and the activity information used by the Vivado power report.

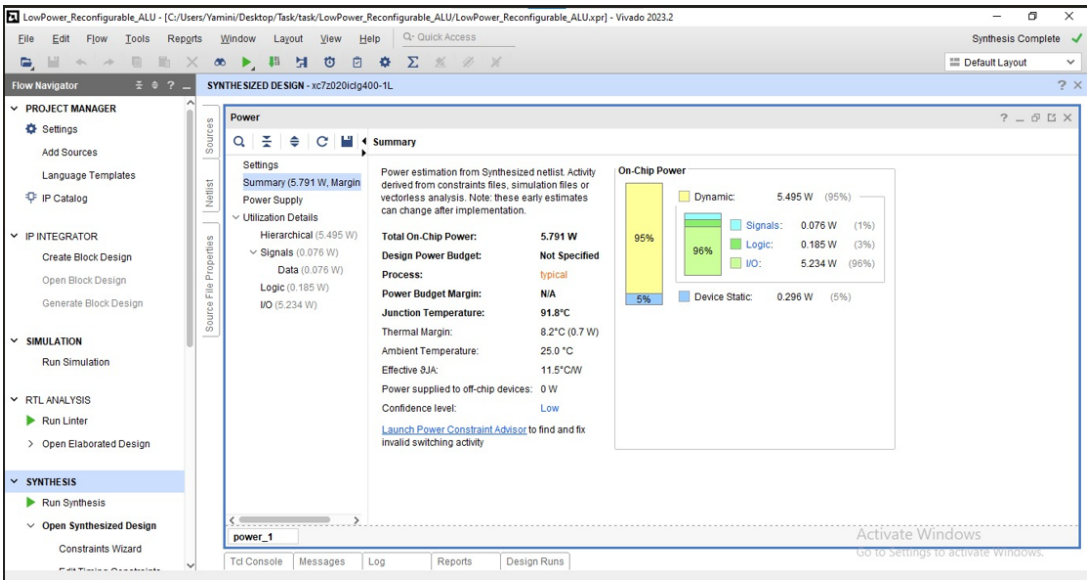


Figure 3: Vivado power report for the conventional 8-bit ALU: Total On-Chip Power = 5.791 W.

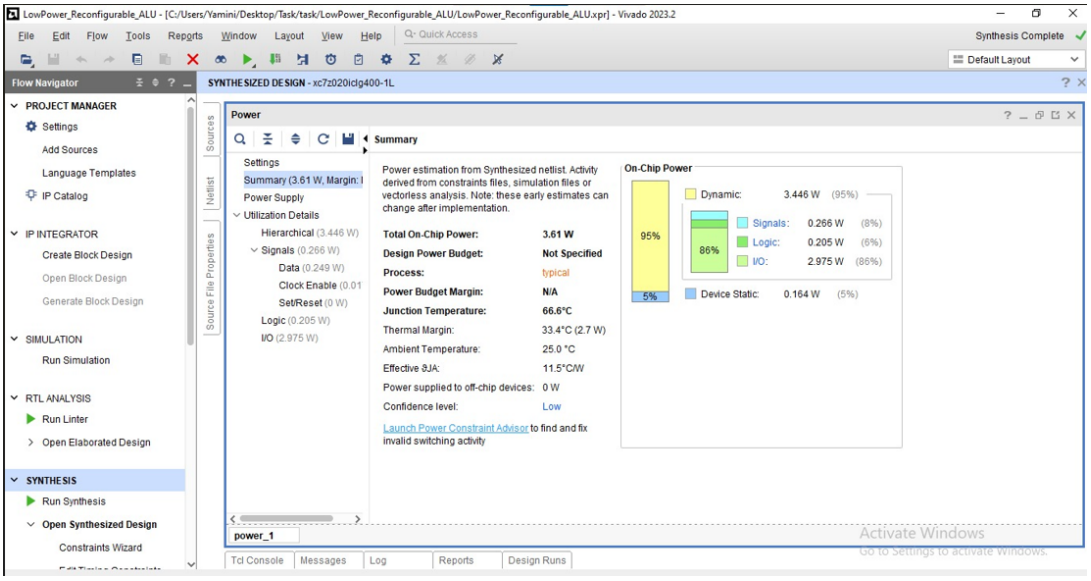


Figure 4: Vivado power report for the fine-grained clock-gated ALU: Total On-Chip Power = 3.610 W.

Table 3: Power Comparison

Parameter	**Conventional ALU**	**Clock-Gated ALU**	**Improvement**
Total On-Chip Power	5.791 W	3.610 W	37.66% reduction
Dynamic Power	5.495 W	3.446 W	37.29% reduction
Static Power	0.296 W	0.164 W	44.59% reduction

Table 4: Thermal and Logic Power Comparison

Parameter	**Conventional ALU**	**Clock-Gated ALU**	**Improvement**
Junction Temperature	91.8 °C	66.6 °C	25.2 °C lower
Logic Power	0.185 W	0.205 W	0.020 W increase

The total on-chip power reduction is calculated as:

$$\text{Power Reduction} = \frac{5.791 - 3.610}{5.791} \times 100$$

$$\text{Power Reduction} \approx 37.66\%$$

Dynamic power reduction is approximately 37.29%, while static power reduction is approximately 44.59%.

Junction temperature decreases from 91.8 °C to 66.6 °C.

Logic power is slightly higher in the gated report, 0.205 W compared with 0.185 W. Therefore, this metric is reported transparently and is not claimed as a reduction.

11. Signal Analysis

Table 5: Signal Description

Signal	**Width**	**Role**
CLK	1 bit	Reference clock for synchronous operation
RESET	1 bit	Initializes the design
A	8 bit	First operand
B	8 bit	Second operand
Op	3 bit	Selects one of eight ALU operations
Y	8 bit	ALU output result
carry	1 bit	Arithmetic carry output

12. Results and Discussion

The simulation confirms the functional behavior of the 8-bit ALU across the selected operation codes.

The final FF + 01 test produces

$$Y = 00$$

with

$$carry = 1$$

confirming the arithmetic carry behavior.

The power reports show a substantial reduction in total on-chip power after introducing the clock-gating approach.

The reduction in dynamic power is consistent with the intended reduction in unnecessary switching activity.

The power screenshots also show a reduction in I/O power in the gated design, while logic power itself is slightly higher. Therefore, the strongest project-level claim is the measured reduction in total and dynamic on-chip power.

13. Comparison of Conventional and Gated Designs

The comparison demonstrates that the proposed low-power approach improves the overall reported power profile under the same Vivado analysis flow.

The total power falls by approximately 37.66%, which is the main quantitative result of this project.

14. Reason for eSim Migration

The next stage of the work is to migrate the verified ALU design to eSim after approval.

The purpose is to reproduce the digital design in an open-source EDA environment, document its operation and clock-gating structure, and provide a reusable implementation for educational and research purposes.

The Vivado measurements are treated as the initial reference results. eSim power behavior should be measured independently during the migration rather than assumed to be identical.

15. Conclusion

An 8-bit reconfigurable ALU using fine-grained clock gating was successfully designed, simulated, synthesized and power-analyzed in Vivado.

The functional waveform verifies the selected ALU operations and the carry condition for FF + 01.

Compared with the conventional implementation, the clock-gated design reduces total on-chip power from 5.791 W to 3.610 W, corresponding to approximately 37.66% power reduction.

Dynamic power decreases by approximately 37.29%, static power decreases by approximately 44.59%, and junction temperature decreases by 25.2 °C.

Although logic power is slightly higher in the gated report, the overall on-chip power reduction demonstrates the effectiveness of the proposed low-power strategy.

The completed Vivado work provides a validated starting point for the planned eSim migration and subsequent open-source implementation.

16. Future Work

Future work includes:

1. Implementing the verified architecture in eSim.
2. Reproducing the functional waveforms.
3. Analyzing the clock-gating behavior in the open-source environment.
4. Comparing resource utilization.
5. Evaluating power under equivalent simulation and activity conditions.

17. References / Project Context

The organization of this report follows the structure of the reference research-migration proposal provided for this project, including sections for theory, architecture, eSim motivation, expected results, signal analysis and migration context.

The present report uses the project's own ALU design and Vivado measurements.

1. Primary tool used: Xilinx Vivado 2023.2.
2. Target device: xc7z020clg400-1.
3. Proposed migration platform: eSim.