RESEARCH MIGRATION PROJECT

A Project Proposal

Design and Optimization of Bootstrapped Switch with Reduced Charge Injection and High Linearity

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1. Title of the Circuit

"Modified Bootstrapped Switch with Reduced Charge Injection and Improved Linearity"

2. Theory / Description

A bootstrapped switch is used in high-speed and high-resolution ADCs to achieve highly linear signal sampling. The Razavi bootstrapped switch maintains an approximately constant VGS, thereby reducing the variation in switch ON resistance. However, charge injection and clock feedthrough during switch turn-off introduce errors in the sampled signal. This project proposes a modified Razavi bootstrapped switch with a dummy NMOS for charge-injection cancellation. The circuit will be designed and optimized to minimize sampling error while preserving high linearity. The proposed design will be simulated using LTspice/eSim and compared with the conventional Razavi architecture. Performance will be evaluated in terms of linearity, charge injection, sampling error, and switching performance.

3. Mathematical Analysis of the Bootstrapped Switch

To analyze tracking behavior, the on-resistance (Ron) of the primary NMOS sampling transistor is expressed as follows:

$$Ron = 1 / [\, \mu * Cox * (W/L) * (VGS - Vth) \,] \quad \text{(Eq. 1)}$$

In a conventional sampling circuit, VGS fluctuates heavily with the input waveform (VGS = Vgate - Vin), producing strong harmonic distortions. The Razavi architecture eliminates this variation by anchoring VGS. During the tracking phase, the gate voltage tracks the input with a fixed VDD offset:

$$Vgate \approx Vin + VDD \quad \text{(Eq. 2)}$$

Substituting Eq. 2 into Eq. 1 cancels out the dynamic input voltage term from the denominator, stabilizing the resistance profile to:

$$Ron \approx 1 / [\, \mu * Cox * (W/L) * (VDD - Vth) \,] \quad \text{(Eq. 3)}$$

4. Mathematical Formulations of Charge Injection and Sampling Error

When the sampling transistor transitions to the off-state, the dynamic channel charge (Qch) held in the inversion layer flows out. The total inversion layer charge accumulated during the tracking phase is defined by:

$$Qch = W * L * Cox * (VGS - Vth) = W * L * Cox * (VDD - Vth) \quad \text{(Eq. 4)}$$

Assuming a distribution factor (γ) describes the fraction of charge spilling onto the hold capacitor (CH), the resulting voltage offset error is given by:

$$\Delta V\_error = \Delta V\_ch + \Delta V\_ft = - (\gamma * Qch) / CH - [\, Cov / (Cov + CH) \,] * VDD \quad \text{(Eq. 5)}$$

Where Cov is the parasitic gate overlap capacitance driving clock feedthrough. To counteract this, a dummy NMOS device featuring half the primary channel width (W_dummy = W/2) with shorted

source/drain junctions is placed at the node. Controlled by the complementary clock phase (CKB), the charge drawn in by the dummy switch is modeled by:

$$Q_{dummy} = W_{dummy} * L * C_{ox} * (V_{DD} - V_{th}) = (W / 2) * L * C_{ox} * (V_{DD} - V_{th}) \quad \text{(Eq. 6)}$$

Since the shorted dummy structure naturally absorbs exactly half of the total channel charge split from the primary device, the overall sampling charge error is neutralized:

$$Q_{net} = \gamma * Q_{ch} - Q_{dummy} \approx 0 \quad (\text{for } \gamma = 0.5) \quad \text{(Eq. 7)}$$

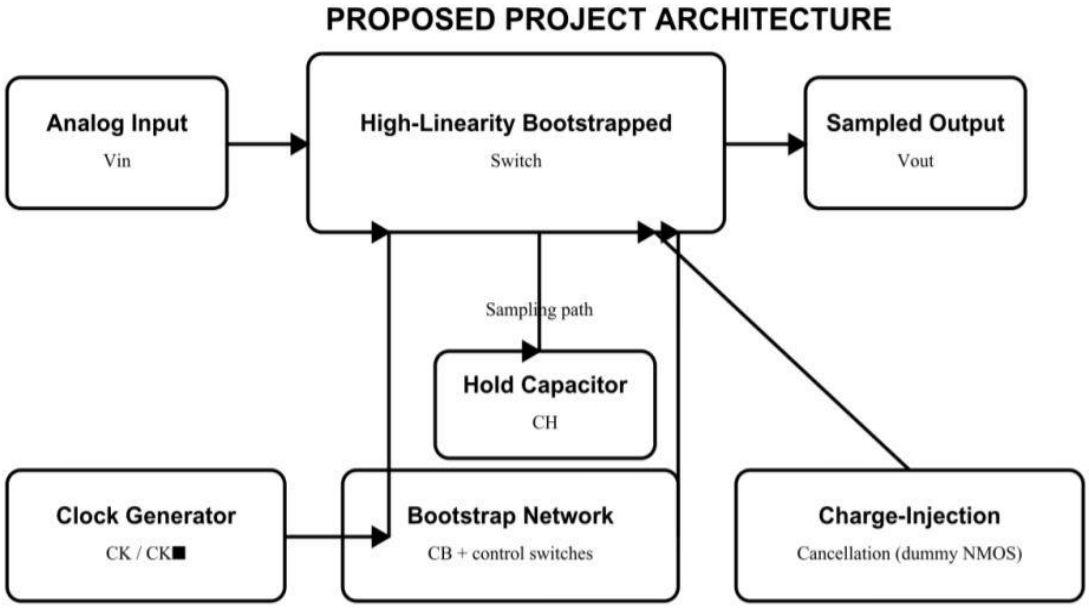
5. Optimization of the Bootstrapped Switch

The proposed optimization modifies the conventional Razavi bootstrapped switch by incorporating a dummy NMOS transistor near the sampling switch to reduce charge injection during turn-off. The dummy transistor is designed to inject a compensating amount of charge opposite to the charge introduced by the main sampling transistor. This minimizes the voltage error on the sampling capacitor and improves sampling accuracy. The transistor sizing and bootstrap capacitor values will also be optimized to achieve a suitable trade-off between linearity, charge injection, settling time, and power consumption. The optimized circuit will be simulated and compared with the original Razavi design to verify the improvement in overall sampling performance.

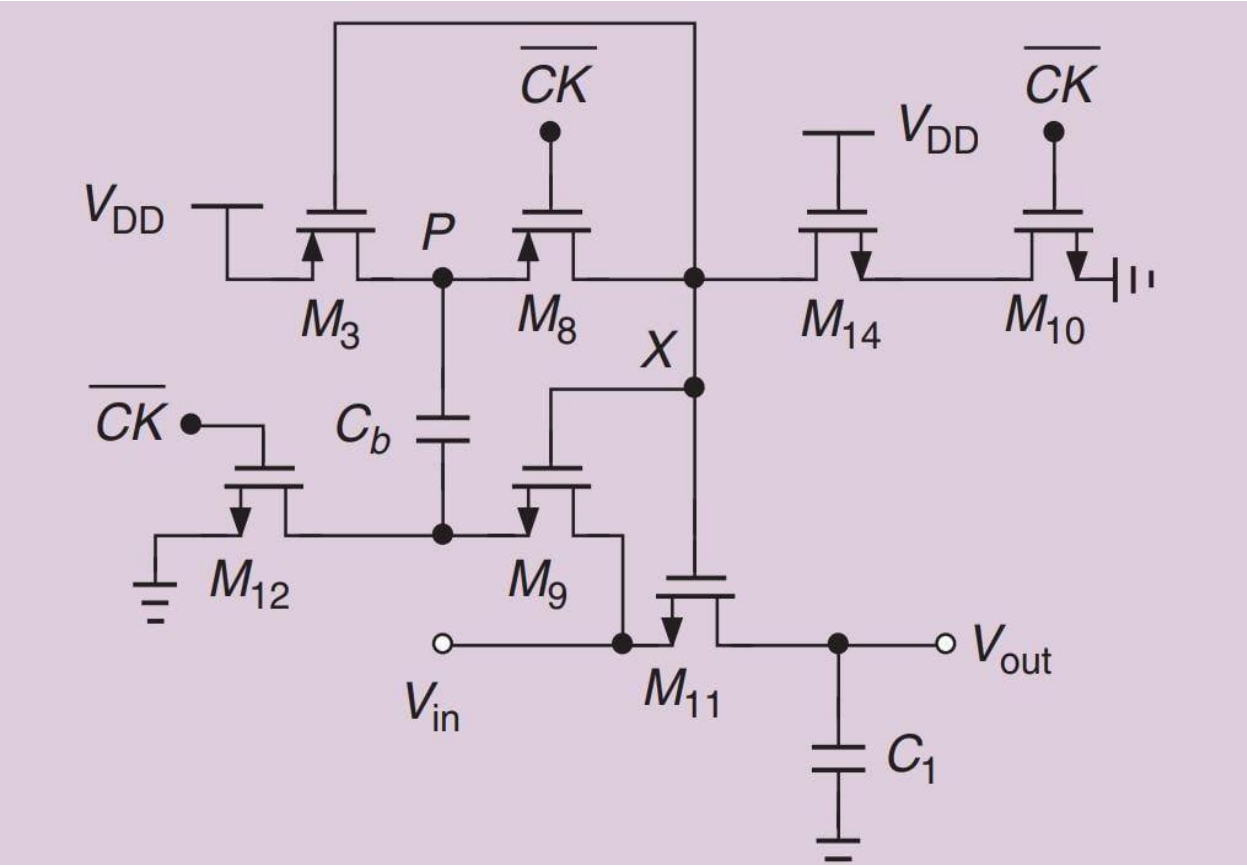
6. Architecture and Working Principle

The proposed architecture consists of a main NMOS sampling transistor, bootstrap capacitor, clock-controlled charging and switching network, and a dummy NMOS for charge-injection cancellation. During the sampling phase, the bootstrap capacitor is charged and subsequently boosts the gate voltage of the sampling transistor, maintaining an approximately constant VGS. This results in a nearly constant ON resistance and improves sampling linearity. During the hold phase, the sampling transistor is turned OFF, causing unwanted channel charge to be injected into the sampling capacitor. The dummy NMOS provides a compensating charge to reduce the net charge injection and sampling error. The transistor dimensions and bootstrap capacitor are optimized to achieve improved linearity, reduced charge injection, faster settling, and lower power consumption.

7. Block Diagram



Initial bootstrapped switch:



Updated Bootstrapped Switch (With Dummy NMOS Insertion)

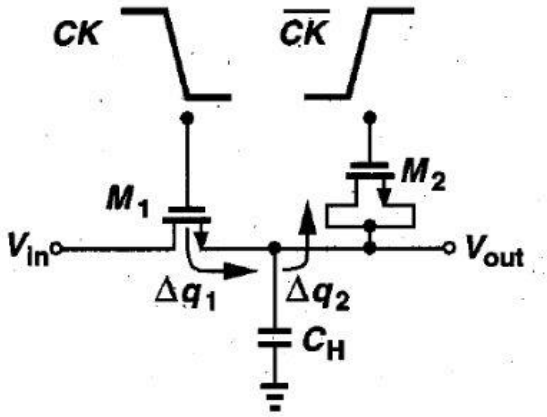
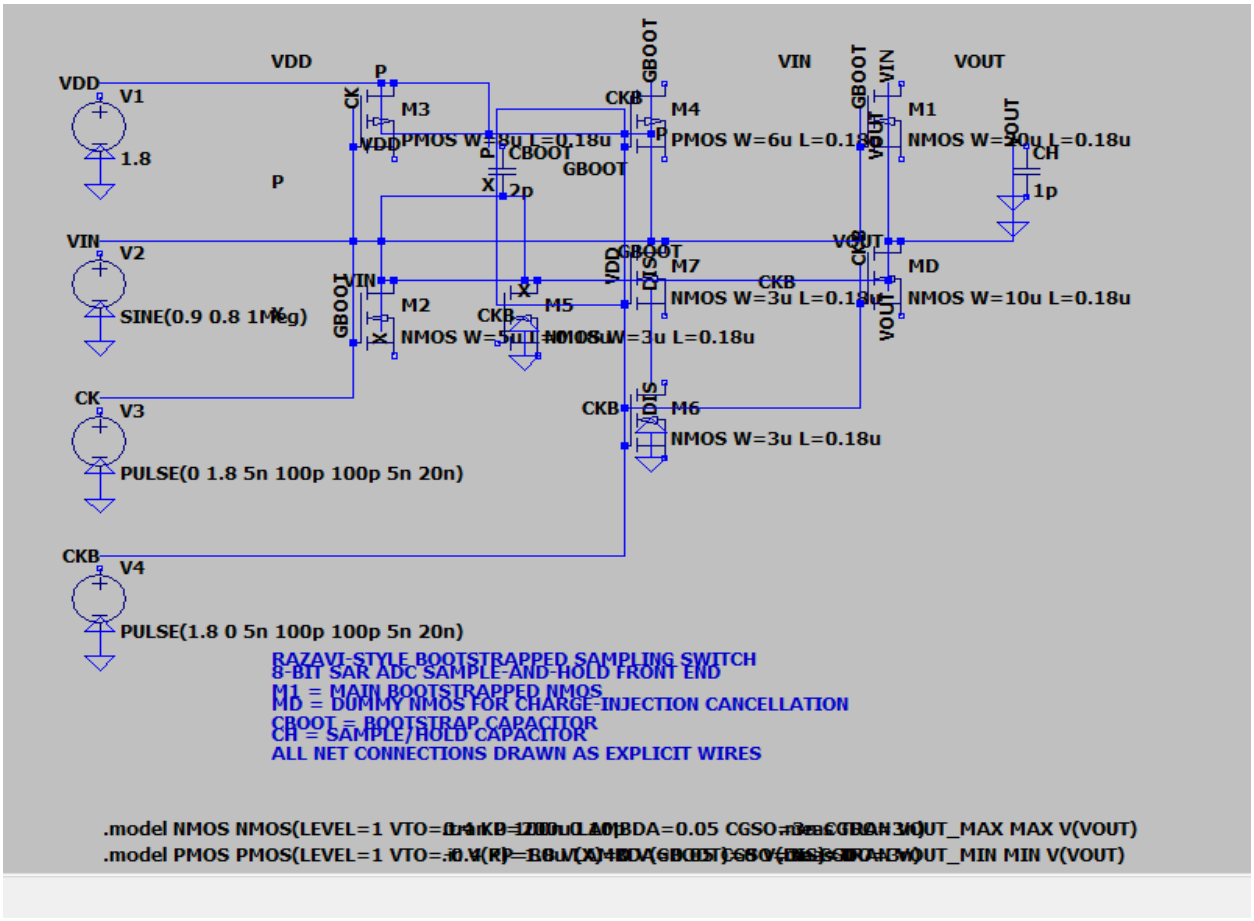
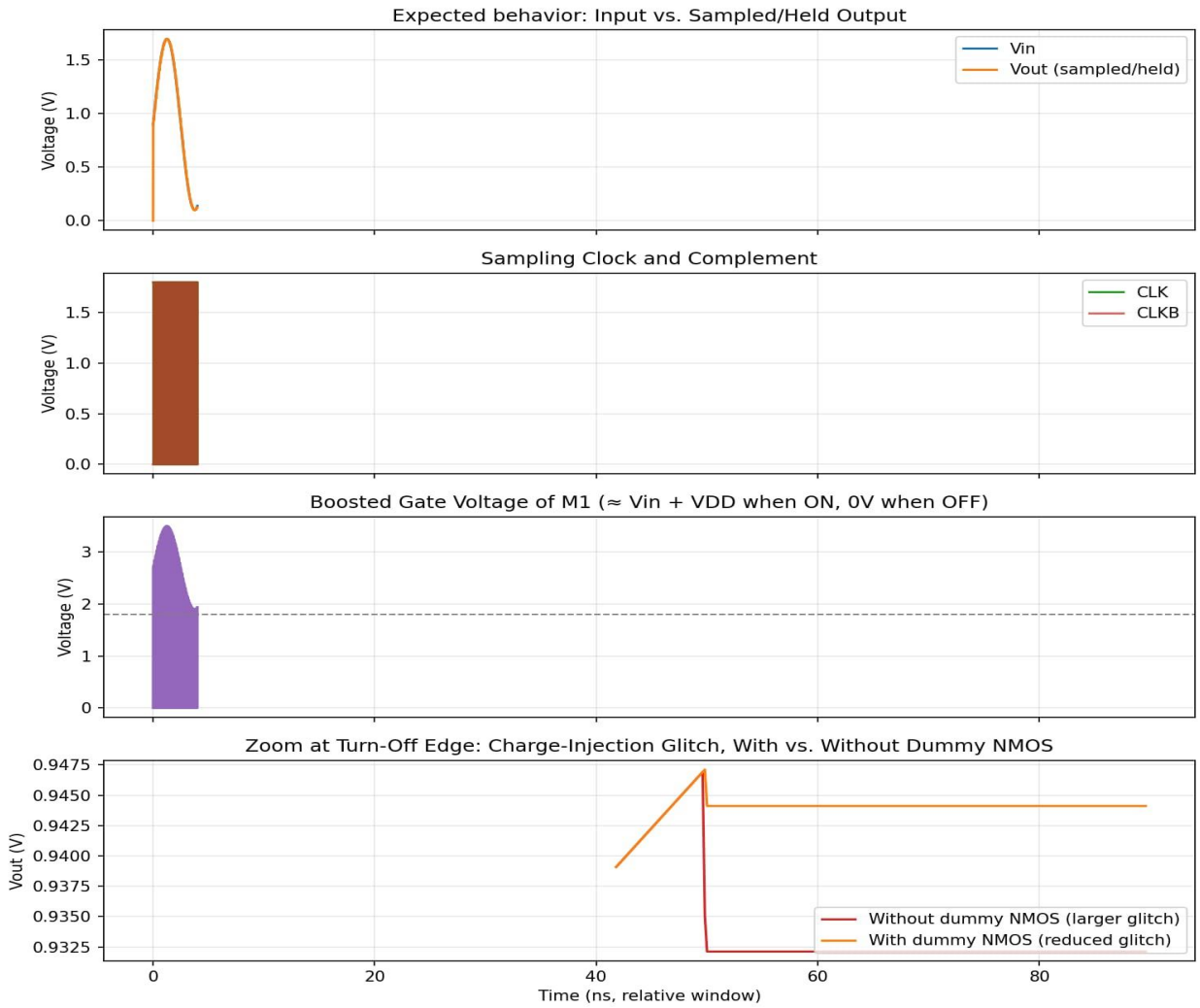


Figure 12.24 Addition of dummy device to reduce charge injection and clock feedthrough.

spice connections:



9. Expected Results



10. Research Paper / Journal

Title: The Bootstrapped switch [a circuit for all seasons]
Author: Behzad Razavi
Affiliation: Electrical Engineering Department, University of California, Los Angeles, California USA
Verified Paper Link: https://ieeexplore.ieee.org/document/7258484