Research Migration Project

https://esim.fossee.in/research-migration-project

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Title of the circuit : Design and Simulation of Parallel CRC Using Pipelining, Unfolding and Retiming

Theory/Description : Conventional serial CRC circuits process one bit per clock cycle, creating a major throughput bottleneck in high-speed systems. This design overcomes that latency by applying unfolding, pipelining, and retiming to process multiple bits in parallel each cycle while systematically balancing register positions to minimize critical path delay. Together, these VLSI transformations roughly halve frame computation time while maintaining high operating frequencies and low gate complexity.

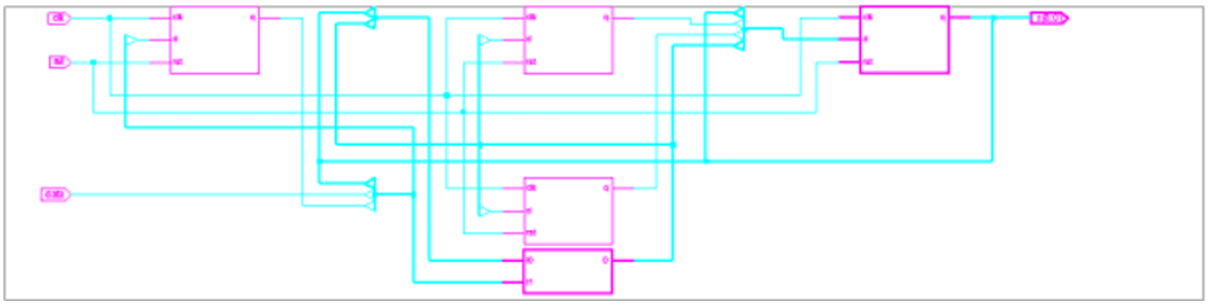
Reason to reproduce with eSim : This project is reproduced using eSim to validate the platform's mixed-signal co-simulation capability, enabling the integration of custom synthesizable Verilog RTL models with the analog SPICE engine through discrete ADC and DAC bridging interfaces. It successfully migrates proprietary HDL simulation benchmarks to a fully open-source EDA toolchain, enriching the FOSSEE repository while demonstrating hardware-level digital state verification alongside standard 0–5 V voltage rails without requiring commercial licenses.

Expected Outcome/outputs : Latency Reduction: Processing a standard 10-bit test sequence (1100000011) settles in 5 clock cycles (20-120ns), compared to 9 cycles for a serial LFSR architecture.

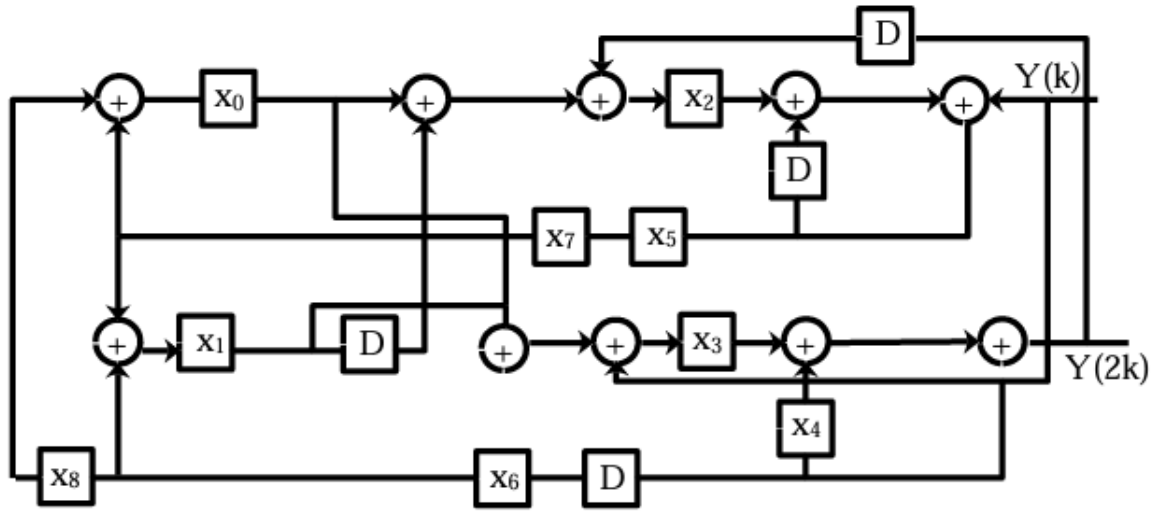
Exact Remainder Convergence: The 9-bit output register vector [x_8 … x_0] updates each clock edge and reaches the final steady-state remainder value 9'b010000001 (0x081) at Cycle 5 (T = 100-120ns).

Signal Integrity: Output traces transition cleanly between standard digital voltage rails (0V for logic 0 and 5V for logic 1) across all parallel registers without transient glitches.

Circuit Diagram(s) :



Block Diagram (s) :



Expected Results (Input, Output waveforms and/or Multimeter readings) :

Research Paper/Journal/etc. : VLSI Implementation of Parallel CRC Using Pipelining, Unfolding and Retiming

Author : Sangeeta Singh, S. Sujana, I. Babu, K. Latha

Link :

https://www.researchgate.net/publication/271250418_VLSI_Implementation_of_Parallel_CRC_Using_Pipelining_Unfolding_and_Retiming